Low Temperature Processing of Printed Oxide Transistors

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Abstract

Solution processed/printed electronics have gained a lot of attention in recent years because they are inexpensive, easy to fabricate, can be produced on very large areas and on all kinds of substrates. The choice of suitable functional/active materials that can be printed is of essential for the performance of the electronic devices in printed electronics. In case of printed field-effect transistors (FETs), which are elemental building blocks of most logic circuits, the right choice of solution-processable semiconductors is the key to obtain high performance electronic devices. In this regard, inorganic oxide semiconductors are considered as a suitable material, because of their excellent electronic transport properties, i.e., high intrinsic charge carrier mobility, in combination with the high thermal and environmental stability. In the design of FETs, apart from the semiconductors, gate insulators/dielectrics play a crucial role. In the present thesis, printable composite solid polymer electrolyte (CSPE) is chosen as gate insulator due to its high capacitance (1-10 $\mu F/cm^2$). Furthermore, CSPEs provide extremely conformal interfaces to the rough oxide semiconductor channel layer, which is the key for high gating efficiency and exceptional device performance.

Two different approaches, i.e., oxide precursors and nanoparticle dispersions, are used to print the semiconductor channels of FETs. The FETs are prepared from appropriate indium oxide precursors, which are annealed at different temperatures (300-500 °C) to be converted to the oxide; however, the devices need to be heated to 400 °C in order to achieve the best electrical performance characterized by a field effect mobility as high as 126 cm^2/Vs and a sub-threshold slope of 68 mV/decade, which is close to the theoretical limit. Furthermore, the effect of the annealing rate on the performance of FETs has been studied. In addition to the single components (FET), complementary metal oxide semiconductor (CMOS) inverters and common source amplifiers have been prepared following a similar fabrication route using indium oxide and copper oxide precursors (annealed at 400 °C). The CMOS inverters have demonstrated a very high signal gain of 21 at 1.5 V. As a second approach and avoiding high processing temperatures, a novel chemical curing method for nanoparticles has been adopted, resulting in a field-effect mobility value of 12.5 cm^2/Vs, strikingly high for a nanoparticulate channel completely processed at room temperature (RT). CMOS inverters based on chemically cured indium oxide and copper oxide nanoparticle dispersions have been prepared, which show a signal gain of 18 at 1.5 V. Another novel technique, i.e. photonic curing, has also been used to fabricate printed FETs on plastic substrates at low temperatures. Precursor-based FETs cured by UV-laser and UV-visible light demonstrate mobility values of 15 and 50 cm^2/Vs, whereas nanoparticulate-based FETs by the same methods show mobilities of 12 and 8 cm^2/Vs, respectively. These values in comparison with those of organic semiconductors verify the outstanding performance of FETs processed at low temperatures (in some cases, even at RT). Furthermore, the low operating voltages ($\leq$ 2V) can be very attractive for battery compatible and portable electronic devices.

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List of Abbreviations

AE	Auxiliary electrode
AFM	Atomic force microscopy
Ag	Silver
AgCl	Silver chloride
Al_2O_3	Aluminium oxide
Au	Gold
BCC	Body centered cubic
BE	Binding energy
BJT	Bipolar junction transistor
BSE	Back scattered electrons
Cd	Cadmium
CE	Counter electrode
CMOS	Complementary metal oxide semiconductor
Cr	Chromium
CSPE	Composite solid polymer electrolyte
Cu	Copper
$Cu(NO_3)_2$	Copper nitrate
Cu_2O	Cupric oxide
CuO	Cuprous oxide
CV	Cyclic voltammetry
DMSO	Dimethyl sulfoxide
DP	Diffraction pattern
EAL	Effective attenuation length
ECT	Electrochemical transistor
EDL	Electrical double layer
EDLT	Electrical double layer transistor
EDS	Energy dispersive spectroscopy
EELS	Electron energy loss spectroscopy
FB	Flat band
FET	Field effect transistor
FFT	Fast fourier transforms
FIB	Focused ion beam
GIS	Gas injection ion beam system
He	Helium

HFET	Heterojunction field effect transistor
HfO_2	Hafnium oxide
HOMO	Highest occupied molecular orbital
IGFET	Insulating gate field effect transistor
IGZO	Indium gallium zinc oxide
$In(NO_3)_3$	Indium nitrate
$In(OH)_3$	Indium hydroxide
In_2O_3	Indium oxide
$InCl_3$	Indium chloride
InOCl	Indium oxychloride
IS	Impedance spectroscopy
ITO	Indium tin oxide
IZO	Indium zinc oxide
JFET	Junction field effect transistor
KrF	Krypton fluoride
$LiClO_4$	Lithium perchlorate
MESFET	Metal insulator field effect transistor
Mo	Molybdenum
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
N_2H_4	Hydrazine
NaCl	Sodium chloride
NDR	Negative differential resistance
NiO	Nickel oxide
NM	Noise margin
NM_H	Noise margin high
NM_L	Noise margin low
NMOS	n-type metal oxide semiconductor
NP	Nanoparticles
PAANa	Poly (acrylic acid sodium salt)
PC	Propylene carbonate
PE	Printed electronics
PEN	Polyethylene naphthalate
PET	Polyethylene terephthalate
PMOS	p-type metal oxide semiconductor
PPC	Parallel plate capacitor

Pt	Platinum
PTFE	Polytetrafluoroethylene
PVA	Poly vinyl alcohol
PVDF	Polyvinylidene fluoride
RE	Reference electrode
RFID	Radio frequency identification tags
RT	Room temperature
SE	Secondary electrons
SEM	Scanning electron microscopy
SiO_2	Silicon dioxide
SnO	Tin monoxide
SS	Subthreshold slope
Ta_2O_5	Tantalum oxide
TEA	Triethanolamine
TEM	Transmission electron microscopy
UHV	Ultra high vacuum
UV	Ultra violet
VIS	Visible
WE	Working electrode
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction
ZnO	Zinc oxide
ZTO	Zinc tin oxide
$\|Z\|$	Modulus of impedance
°C	Degree centigrade
μ_{FET}	Field effect mobility
µm	Micrometer
A	Ampere
C	Capacitance
C_D	Capacitance of depletion layer
C_{dl}	Double layer capacitance
cm	Centimeter
d	Distance
D	Drain
E	Potential
eV	Electron volt
F	Farad

G	Gate
G_m	Transconductance
h or hr	Hour
I	Current
I_D	Drain current
I_{DD}	Supply current of CMOS
I_G	Gate current
k	Boltzmann's constant
K	Kelvin
l	Characteristic length of a nozzle
L	Length
ln	Natural logarithm
m*	Effective mass
mA	Milliampere
min	Minute
nA	Nanoampere
nm	Nanometer
Oh	Ohnesorge number
pA	Picoampere
q	Charge
S	Source
s or sec	Second
T	Temperature
T_m	Mean free time
V	Voltage
V_D	Drain voltage
V_{DD}	Drain voltage of CMOS
V_{FB}	Flat band voltage
V_G	Gate voltage
V_{IH}	Minimum high input voltage
V_{IL}	Maximum low input voltage
V_{IN}	Input voltage of CMOS
V_{OH}	Minimum high output voltage
V_{OL}	Maximum low output voltage
V_{OUT}	Output voltage of CMOS
V_T	Threshold voltage

W	Width
z	Dimensionless number of printing
Z	Impedance
Z'	Real part of the impedance
Z''	Imaginary part of the impedance
γ	Surface tension
η	Viscosity
λ_m	Mean free path
ρ	Density

1. Motivation

We are living in an "Electronic age": from the day vacuum tubes were invented, the revolution in electronics took-off. Vacuum tubes were extensively used in radios, televisions, radar systems, etc. until the 1980's. However, the actual modernization of electronics took place after the discovery of solid state field-effect devices, i.e., the transistor, by John Bardeen, William Shockley and Walter Brattain in 1947. In the wake of this discovery, revolutionary new developments were accelerated to realize many indispensable gadgets such as communication systems (phones, computers, etc.), entertainment systems (televisions, musical instruments), medical appliances, defense related instruments, and more systems in many other fields [1]. Along with regular applications, new technologies evolved during every decade, which were not imaginable a few years before. In this way, as the technology is growing, new application needs develop; one of the most recent one is printable, flexible, disposable and transparent electronics. For the realization of printed electronics, suitable materials and optimized processes or techniques need to be identified or developed. In this regard, organic materials (molecules and polymers) have always been the first choice because they can easily be prepared by solution processes at low temperatures, and are mechanically flexible and inexpensive. However, after extensive studies over many years, the open problems of limited environmental stability and rather low values of electron mobility have persuaded scientists to look for alternative materials. Carbon-based or inorganic semiconductors have most commonly been investigated. In fact, both crystalline (indium oxide (In_2O_3), zinc oxide (ZnO), tin oxide (SnO_2), etc.) and amorphous oxide semiconductors (indium gallium zinc oxide (IGZO), zinc tin oxide (ZTO), indium zinc oxide (IZO), etc.) have certain advantages compared to organics such as their high stability in ambient conditions as well as at high temperatures, ease of manufacture by most of the available techniques, high intrinsic mobility values (in fact, orders of magnitude higher when compared to organic semiconductors), transparency for visible light due to high band gap, etc. [2-7]. As typically solutions are available, printing is versatile and offers plenty of advantages such as ease of use and applicability to large areas and volumes. Furthermore, printing is inexpensive and can be roll-to-roll, non-contact, mask-less, non-vacuum, and actually it is substrate independent, i.e. almost all kinds of rigid and flexible substrates can be employed [8-10].

Transistors are the essential building blocks of most electronic circuitry. The active elements of a transistor are the semiconducting layer called channel and the dielectric or gate insulator layer that polarizes the semiconducting layer. As mentioned above, nontoxic, inexpensive and easy to fabricate oxide semiconductors are good candidates for solution-processed flexible electronics. Typically, conventional oxide insulators, such as silicon dioxide (SiO_2), aluminium oxide (Al_2O_3), or oxide insulators with high dielectric constants (typically known as high-k dielectrics), such as hafnium oxide (HfO_2), tantalum oxide (Ta_2O_5), etc., have been considered as gate dielectrics. However, for solution processed FETs, these inorganic materials are often not suitable for the following reasons. Typically, high temperatures are required for the formation of the desired insulating phase.

Solution processing, preferably used for preparing nanoparticulate films are characterized by a high porosity, which influences the device performance and causes leakage currents through the dielectric layer. Most importantly, it is extremely difficult to obtain smooth interfaces between the dielectric and the semiconductor layers, an interface of utmost importance for the transistor performance. In this thesis, the possibility of using a solid polymer electrolyte as the gate insulator has been explored as an alternative to the standard dielectric concept. Typically, electrolytes contain ions, which form an electrical double layer (EDL) at the electrode or semiconductor-electrolyte interface upon application of a potential. With the selection of the correct potential window, one can nearly eliminate the presence of any unwanted redox reactions at the interface. Therefore, electrolyte gating becomes highly analogous to the well-established dielectric gating mechanism which uses an oxide insulator. In addition, for the case of electrolyte gating a high capacitance (due to the EDL) can be obtained, resulting in low operating voltages. Electrolytes can be easily prepared by solution processes and transform into a solid after the evaporation of the solvent during drying. As a result, an all-solid-state device is obtained [11-13]. The combination of electrolyte gating of inorganic semiconductor layers is considered as an interesting alternative to dielectric gating of organic semiconductors for the case of flexible electronics. The various possible combinations of oxide semiconductors and electrolytes as insulators offer very high performance FETs, even when processed using standard printing techniques. In the present thesis, this combination of a novel composite solid polymer electrolyte and solution processed/printed oxide semiconductor layers is presented. As a proof of principle, single FET devices and simple logics, which are processed at low or even room temperatures, as the primary building blocks of electronic circuits are presented.

The contents of the research program of the thesis are structured in the following chapters as follows. Chapter 2 provides a literature review on different topics such as field-effect transistors, CMOS, oxide semiconductors, electrolyte-gating, solution processed/printed FETs, inkjet printing, oxide nanoparticle dispersion versus precursor routes for fabrication of printed oxide FETs, etc. In addition to a basic introduction to the topic, a brief overview of the state-of-the-art literature results is provided. Chapter 3.1 describes the preparation, electrical characterization and discussion of the precursor-based indium oxide FETs from metal halide precursors. In addition, the effect of the annealing conditions on the performance of oxide FETs is presented. Chapter 3.2 elaborates on the synthesis and characterization of CMOS inverters as well as common source amplifiers using n-type indium oxide and p-type copper oxide precursors. Following the thrive to reduce process temperature, Chapter 4 illustrates the details of room temperature processing of indium oxide nanoparticle-channel FETs following a so-called chemical curing technique. Chapter 5 describes the photonic curing (using UV-laser and UV-pulse units) of precursor-based, as well as nanoparticle-based oxide FETs on glass, as well as on plastic substrates. The last Chapter 6 provides the conclusions and the outlook of the present thesis.

2. Introduction and Literature Review

This chapter presents an introduction and a comprehensive literature review on the relevant topics, such as field-effect transistors, complementary metal oxide semiconductors, oxide semiconductors, solution processing techniques especially inkjet printing, solution processed/printed FETs, concept of electrolyte gating, precursor versus nanoparticle thin film preparation routes, and characterization techniques as well.

2.1. Field-effect transistors

A transistor is a semiconductor based device, which has resulted in a revolution in electronics. In principle a FET is used either for amplifying (analog device, i.e. regulating larger output power than the input) and/or for switching (digital application, i.e. on-and-off state) electronic signals. A transistor is a three terminal device in which the flow of charge carriers (electrons or holes) between two terminals is controlled by a third terminal. The flow of charge carriers can be controlled either by current (bipolar junction transistor, BJT) or by an electric field (field-effect transistor, FET). BJTs consist of both n-type (electrons) and p-type (holes) charge carriers and the best known configurations are n-p-n and p-n-p junctions. On the other hand, FETs are unipolar, i.e. either electrons or holes can be used as the charge carriers. FETs have many advantages over BJTs such as high input impedance, negative temperature coefficient at higher currents, higher large-signal switching speeds etc., and in addition, FETs are also thermally stable. FETs have applications both in analog and in digital circuits. FETs are divided into many types based on the manner that the gate capacitor is formed; for example, junction FET (JFET, in which the capacitor is formed by the depletion layer of a p-n junction), metal-semiconductor FET (MESFET, in this case, a Schottky barrier acts as the gate capacitor), and insulated gate FET (IGFET), etc. IGFETs are again divided into different types, such as, metal oxide semiconductor FET (MOSFET, metal oxide is used as the gate capacitor), heterojunction FETs (HFET, heterojunction formed from a high bandgap semiconductor acts as the gate capacitor), etc. Among all these, MOSFETs have gained special attention because they can be operated either in enhancement (normally-off) or in depletion mode (normally-on), they are easy to fabricate, possess relatively higher switching speeds, and high input impedances (which leads to lower leakage currents), etc. Among all these different FETs, MOSFETs are extensively used in most electronic applications [14].

In MOSFETs, charge carriers flow from one drive electrode (source) to the other (drain) through a semiconducting channel layer, and this flow of carriers is controlled by an electric field applied at the third electrode (gate), which is separated from the channel layer by an oxide or dielectric layer. A typical MOSFET is shown in **Figure 2-1**.

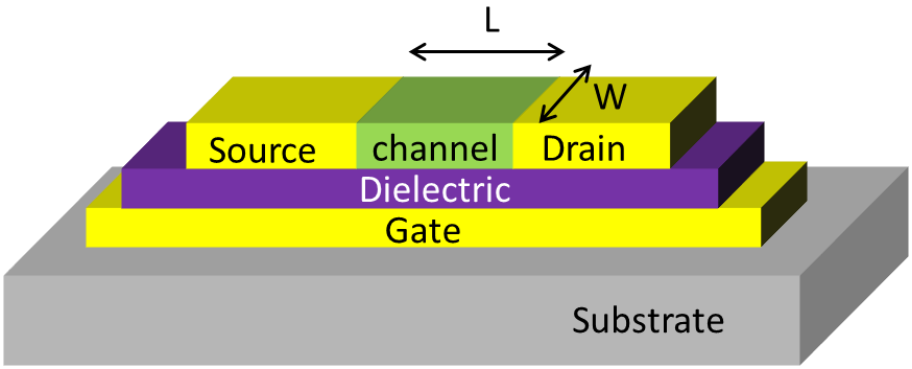

Figure 2-1 Schematic of a bottom gate MOSFET. The stack consisting of gate electrode, insulating dielectric layer, semiconducting channel, source and drain electrodes is shown as deposited on a substrate. Dimensions of importance for the performance of the MOSFET, i.e., channel length (L) and widths (W) are shown in the schematic as well.

For a further explanation of the operation of a typical MOSFET, electrons (i.e. the carriers in case of n-type semiconductors) are considered as the charge carriers in the present case, thereby making it a n-channel MOSFET, commonly known as NMOS. In NMOS, the source is grounded (zero voltage) and voltages are applied at drain and gate electrodes. When a positive voltage is applied at the gate, an electron-rich layer (or simply the channel layer) between source and drain is formed. Electrons start to flow from source to drain through the channel when sufficient voltage is applied at drain. If the drain voltage (V_D) is more than the threshold voltage (V_T is defined as the gate voltage below which the device is in the off-state), then it forms an inversion layer and provides large drain currents (I_D). Sweeping the gate voltage (V_G) with an applied constant drain voltage results in a so-called transfer curve of the FET as shown in **Figure 2-2a**. The ratio of the high and low drain currents gives the ON/OFF ratio of the FET device; for example, in case of **Figure 2-2a**, it is 10^7. From the linear fit of the square root of the drain curve, the threshold voltage is determined as the intersection with the x-axis. Based on the threshold voltage value, i.e. either positive or negative, the device is said to be in either enhancement or depletion mode, respectively.

The output characteristics or current (I) - voltage (V) curves of a typical FET are shown in **Figure 2-2b**. The I-V curves show three regions, namely, linear, non-linear and saturation regions. At low drain voltages, the FET channel behavior is analogous to a resistor. At further increase in the drain voltage, the channel deviates from the resistor-like behavior due to the channel potential build up at the drain end, and finally it saturates because of nearly zero inversion charge at the drain [14]. The drain voltage at which saturation of the drain current starts is called pinch off voltage. The change in the drain current with respect to the gate voltage is quadratic and it is governed by the relationship, $I_D \propto (V_G\text{-}V_T)^2$.

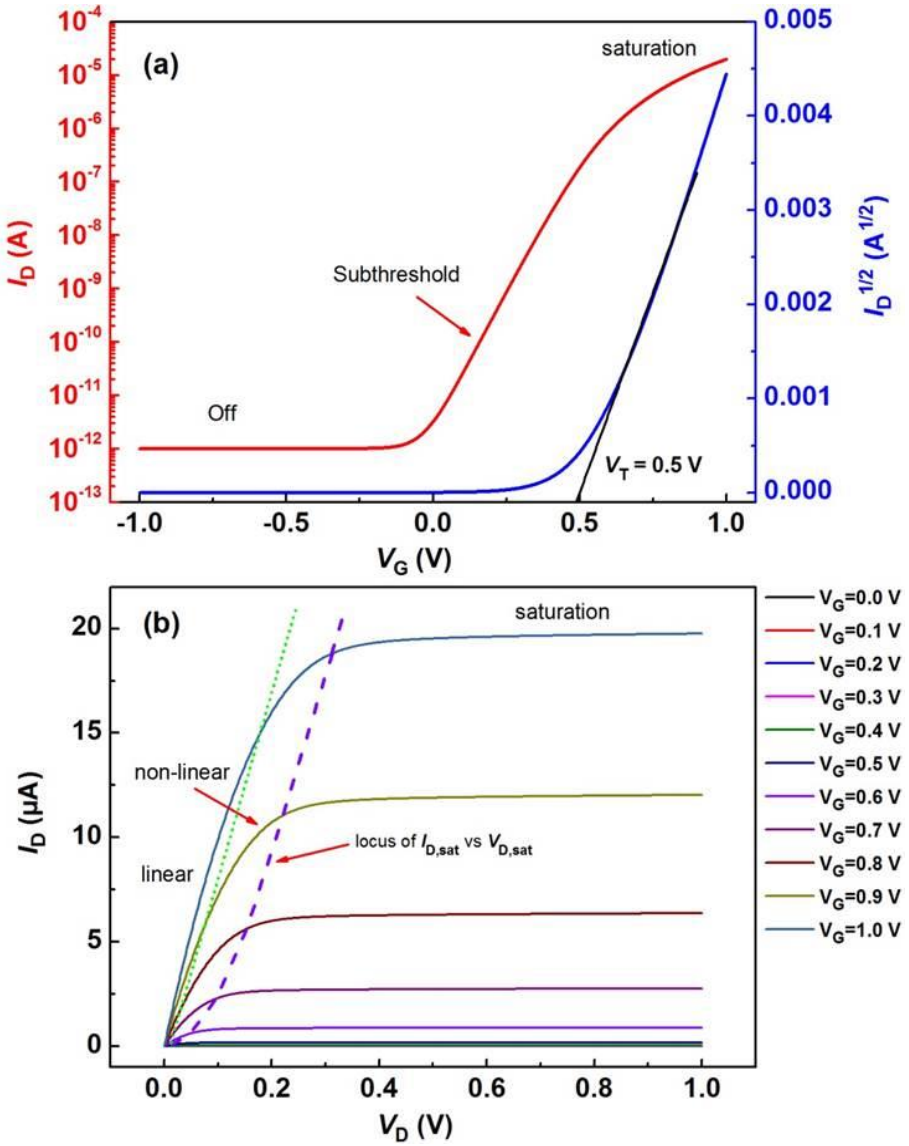

Figure 2-2 (a) Transfer and (b) Current (*I*)-Voltage (*V*) curves of a typical FET. The transfer curve shows the gate voltage (V_G) on the x-axis and the drain current (I_D, red line), the square root of the drain current ($I_D^{1/2}$, blue line) with a linear fit (black line) to obtain the threshold voltage (V_T) are shown on y-axis. The *I-V* curves show the drain voltage on the x-axis and different drain current curves with a variation of the gate voltage on y-axis. Three different regions of the *I-V* curves, i.e. linear, non-linear and saturation regions are also shown.

One of the most important figures of merit of a transistor is the field-effect mobility (μ_{FET}). In general, the intrinsic mobility (μ) depends on the effective mass and the mean free time (τ_m) or the mean free path (λ_m). The governing equation is $\mu=q\tau_m/m^*=q\lambda_m/(3kTm^*)^{1/2}$, where q is charge, m* is effective mass, k is Boltzmann's constant and T is temperature. If all other conditions are identical except the effective mass, electrons can have higher mobility than holes due to their low effective mass. Other than effective mass, the mobility is mainly controlled by scattering phenomena. Scattering can be due to phonons (acoustic, optical and also vibrations due to high temperatures), impurities, grain boundaries, etc. However, intrinsic and field-effect mobility values are slightly different because the latter one is a surface phenomenon. Moreover, the field effect mobility is typically lower than the intrinsic mobility due to higher scattering effects at the semiconductor-dielectric interface. In

other words, this implies that an extremely conformal interface quality between these two would ensure large field effect mobility values, close to the intrinsic mobility value of the single crystal [15]. Therefore, preparing FETs without impurities, with fewer grain boundaries, operating at optimal temperatures, etc. will lead to high mobility FETs. The usual expression to calculate field-effect mobility (when $V_D \geq V_G$-V_T) in the saturation regime involving saturated drain current ($I_{D,sat}$) can be written as:

$$\mu_{FET} = \frac{I_{D,sat} \times 2L}{WC\,(V_G - V_T)^2} \qquad (2.1)$$

However, when $V_D << V_G$-V_T, field-effect mobility is calculated with drain current of linear regime ($I_{D,lin}$):

$$\mu_{FET} = \frac{I_{D,lin} \times L}{WC\,V_D\,(V_G - V_T - \frac{V_D}{2})} \qquad (2.2)$$

where L is length, W is width, C is capacitance. Another important parameter is sub-threshold swing (SS), which indicates how sharply (with respect to gate sweep) a transistor switches off. It is the ratio of change of gate voltage to the change in drain current by one order of magnitude. It is important to know the subthreshold region for low power applications, especially, when it is used as a switch [14]. The equation of subthreshold swing is:

$$ss = (\log_e 10)\left(\frac{KT}{q}\right)(1 + \frac{C_D}{C}) \qquad (2.3)$$

where C_D is the capacitance of the depletion layer. In an ideal case, when C_D is zero, the corresponding SS at room temperature is 60 mV/decade, and this is the theoretical limit of SS.

Another important parameter to define the amplification or gain of a transistor is called transconductance (G_m). For a MOSFET, at a constant drain voltage, it is the ratio of change in the drain current to the change in gate voltage. It can be deduced from the slope of transfer curve (in the linear region) [14]. The equation of transconductance is given as,

$$G_m = \frac{dI_D}{dV_G} \qquad (2.4)$$

2.2. Complementary metal oxide semiconductors

Complementary metal oxide semiconductors (CMOS) are the basic building blocks of logic circuits. CMOS are often used in both analog and digital applications due to their low static power consumption, high noise immunity, short propagation delays, etc. CMOS also increase the speed and packing density of FETs [16]. The CMOS consist of a pair of n-type (NMOS) and p-type metal oxide semiconductor (PMOS) FETs. Out of several CMOS logics (inverter or NOT gate, NAND gate, NOR gate, etc.), CMOS inverter is a simple logic that inverts the input signal. The CMOS inverter generates the high output for a low input and a low output for a high input signal. The circuit diagram of a typical CMOS inverter is shown in **Figure 2-3a**. It shows that the gate and source electrodes of both PMOS and NMOS are connected. The other drive electrode of the NMOS is grounded (V=0) and the supply or drive voltage (V_{DD}) is applied at the PMOS end. While the input voltage (V_{IN}) is applied at the common gate, the output voltage (V_{OUT}) is measured at the common source. The output curve or

voltage transfer curve (VTC) of a CMOS inverter is shown in **Figure 2-3b**. It shows the high output, the transition and the low output regions. The major determining factor of an inverter is the signal gain (dV_{OUT}/dV_{IN}), i.e. how sharp the transition between the high and low output regions takes place. Five distinguishable regions are indicated (A, B, C, D, E) in **Figure 2-3b** for a better understanding. At low input voltages, NMOS is off and PMOS is in the linear mode, which means that there is no voltage drop ($V_{OUT} = V_{DD}$) in region A. As the input voltage increases, PMOS is still in the linear mode, whereas the NMOS starts to switch on: this in return reduces the output voltage in region B. In region C, both FETs are in saturation regime and the voltage reduces to half, i.e $V_{OUT} = V_{DD}/2$. In region D, PMOS is in the saturation mode and the NMOS is in the linear regime. As the voltage increases further (region E), the PMOS switches off and the NMOS is in the linear mode, which completely pulls the output voltage down, i.e. $V_{OUT} = 0$. **Figure 2-3c** shows the supply current (I_{DD}) while the inverter is in operation and the maximum current is drawn at the transition, i.e for region C.

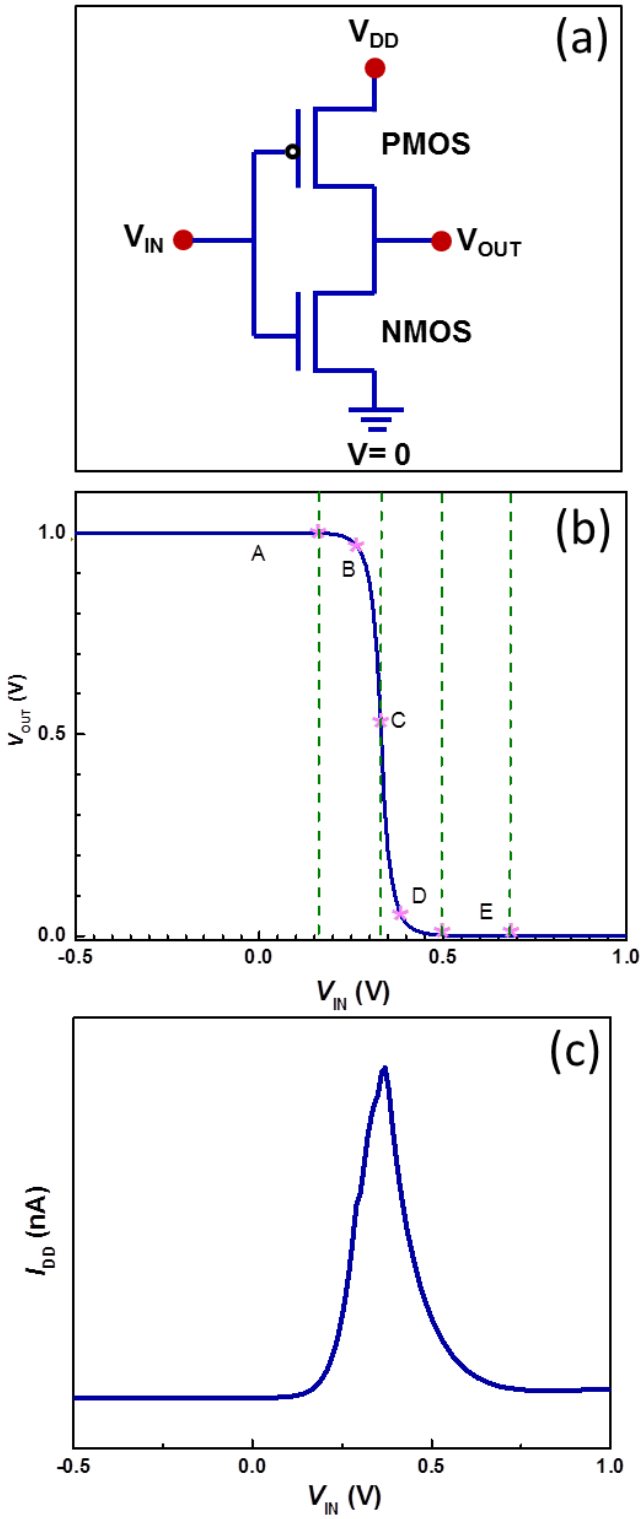

Figure 2-3 CMOS inverter (a) circuit diagram, (b) voltage transfer curve and (c) supply current graph. The circuit diagram shows the combination of NMOS and PMOS transistors with input (V_{IN}), output (V_{OUT}) as well as supply or drive (V_{DD}) voltages. The voltage transfer curve shows high output, transition and low output regions. The supply current graph indicates that the maximum current (I_{DD}) is drawn at the transition region [17].

The noise margin (NM) is one of the determining parameters of an inverter. It indicates the allowable voltage noise on the input, so that the output voltage will not be affected. There are two noise margins that can

be defined, i.e. the high noise margin (NM_H) and the low noise margin (NM_L). Noise margins can be calculated from the transfer curve of the inverter. The calculations and logic diagrams are shown in **Figure 2-4a** and **Figure 2-4b,** respectively. The logic diagrams show three regions i.e. logic 1, indeterminate or forbidden (no logic signal) region and logic 0. It is preferable to have equal noise margin values (or logic range) for NM_H and NM_L and very low forbidden regions. High NMs have better immunity to noises. However, it may be important to note that for some applications, NMs can be compromised to obtain higher switching speed. NMs may also change with drive/input voltages, so it is better to describe them as a fraction of voltage. The equations of high and low noise margins are

$$NM_H = V_{OH} - V_{IH} \qquad (2.5)$$

$$NM_L = V_{IL} - V_{OL} \qquad (2.6)$$

where V_{OH}= minimum high output voltage, V_{IH}= minimum high input voltage, V_{OL}= maximum low output voltage, V_{IL}= maximum low input voltage, respectively [17].

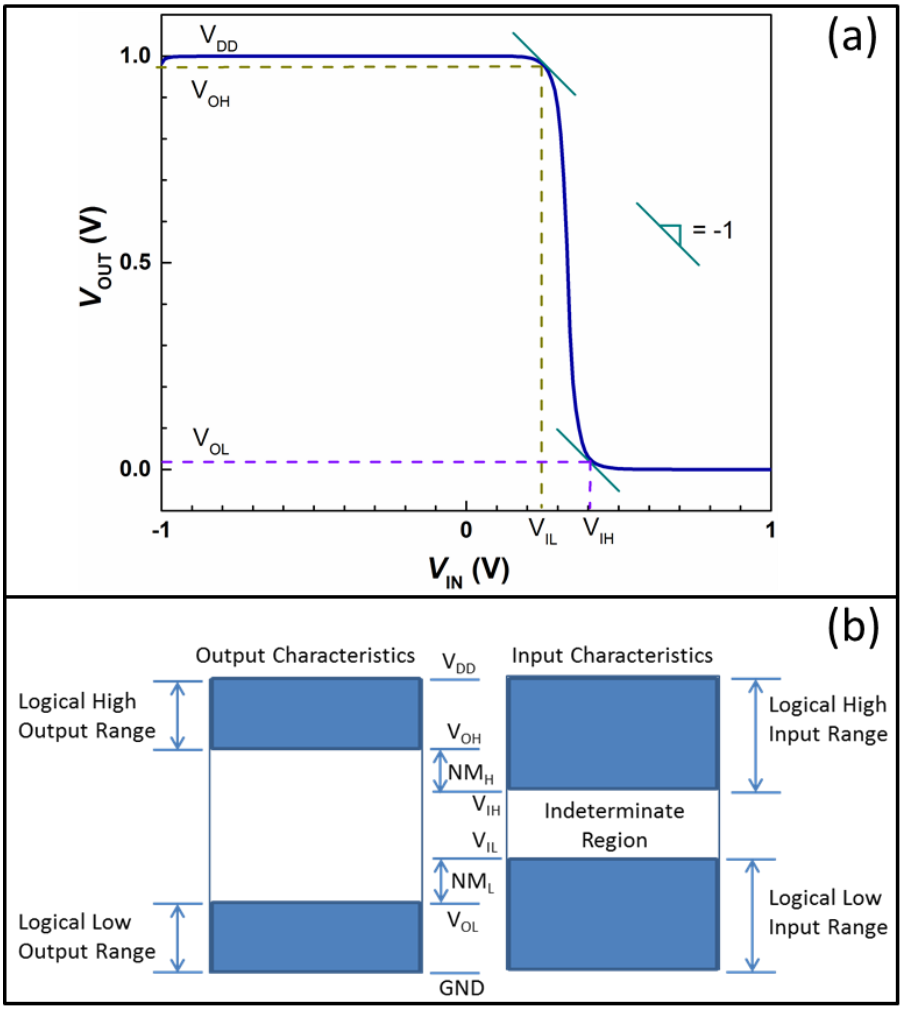

Figure 2-4 CMOS inverter (a) noise margin and (b) logic diagrams. Noise margin diagram shows different input, output voltages from which high as well as low noise margins are calculated. Logic diagram shows the logical high input range, indeterminate and low input ranges [17].

2.3. Oxide semiconductors

The electrical conductivity of semiconductors lies between those of metals and insulators. The electrical properties of semiconductors can be varied by doping, temperature, optical excitation, etc. This makes semiconductors suitable for various applications and has attracted the scientific community to investigate them for various electronic applications [18]. Although, germanium was used as a semiconductor for the first-ever transistor, silicon (Si) replaced it quickly thereafter because of its extremely low cost, large availability, flexibility for doping, etc. Another intriguing factor in favor of silicon is its ability to provide equally good n- and p-type doped counterparts, which is basically the key behind the success of Si-electronics. High quality single crystals and polycrystalline silicon are widely used in integrated circuits and other applications. On the other hand, in recent times, there is a great interest towards large area electronics (e.g. using glass as the substrates) such as liquid crystal displays, medical X-ray imaging devices, etc. For these applications, amorphous silicon is widely used. However, a quest for alternative materials, which can perform better, possible to be produced at lower cost on plastic substrates, is still on. Organic molecules and polymers have been tested for these purposes but certain disadvantages such as low performance, low environmental stability, lack of controlled doping etc. have limited their prospect. On the other hand, crystalline oxide semiconductors such as ZnO, In_2O_3, SnO_2, CuO, Cu_2O, SnO, NiO as well as amorphous semiconducting oxides such as ZTO, IZO, IGZO etc. are found to be suitable materials of choice for numerous applications because of their high intrinsic mobility, optical transparency, and possibility to be produced on large areas also. On top of this, oxide semiconductors can also be solution processed [19]. The semiconducting behavior of these oxides is caused by oxygen vacancies and metal interstitials for n-type and for p-type oxides, respectively. When it comes to band structure, the valence and the conduction bands are formed by the overlap of metal ns and oxygen 2p orbitals, which leads to a highly dispersive conduction band and a localized valence band. Therefore, it causes low effective mass for electrons than holes, which in turn leads to high mobility for n-type oxide semiconductors compared to the p-type ones [20]. Next, several pertinent and interesting example oxide semiconductors, both n- and p-type are discussed in detail.

In_2O_3: It has a body centered cubic bixbyite structure (space group Ia3) with a coordination of 16 molecules per unit cell (80 atoms). This structure has two crystallographically non-equivalent indium sites (named as In(1) and In(2)) and only one type of site for oxygen atoms. Both indium sites are 6-atom coordinated and oxygen sites are 4-atom coordinated. In(1) sites are surrounded by 6 oxygen atoms which lie nearly at the corners of a cube with two body-diagonally opposite corners unoccupied and In(2) sites are also surrounded by 6 oxygen atoms which lie at the corners of a cube with two face-diagonally opposite corners unoccupied [21]. The crystal structure is shown in **Figure 2-5** [22]. The carrier concentration is rather high compared to other oxide semiconductors, i.e. 10^{18}-10^{20} cm^{-3} dependent on doping and preparation conditions [23]. It is an n-type semiconductor with high intrinsic mobility of 160 cm^2/Vs [24], due to its crystal structure in which linear chains

of edge sharing octahedra run isotropically [25]. It also has a high bandgap of 3.75 eV (indirect) [26], which makes it highly attractive for optically transparent applications. In_2O_3 is a thermodynamically highly stable oxide in ambient conditions, and it can be easily prepared by different methods such as physical [27-29] as well as chemical vapor deposition [30-32], wet chemical methods [33-35], etc. It is highly used as a semiconductor in its intrinsic form and also as a metal-like electrode when it is doped with tin (indium doped tin oxide, ITO). All these attractive features make it a suitable candidate for many electronic applications such as displays [36], solar cells [37, 38], smart windows [39], sensors [40, 41], etc.

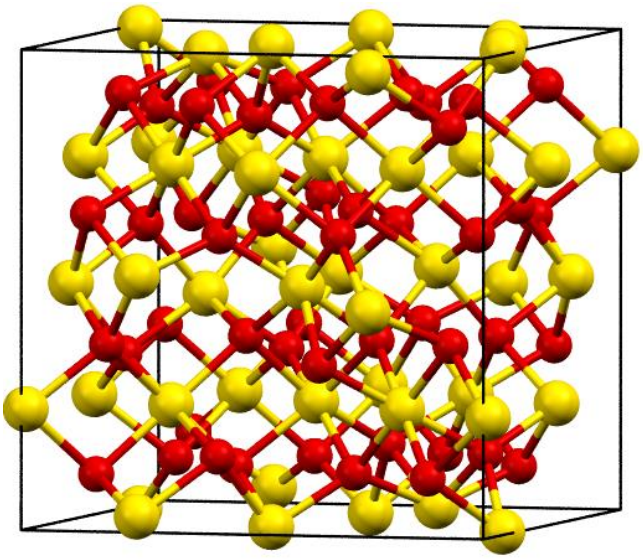

Figure 2-5 Crystal structure of $In_{32}O_{48}$, where indium and oxygen atoms are represented by yellow and red color spheres, respectively. Indium oxide crystallizes in the cubic bixbyite structure [22].

Cupric oxide (CuO): CuO is a p-type semiconductor with a bandgap of 1.2-1.9 eV. It has a monoclinic structure (space group C2/c) with 4 formula units per unit cell; the crystal structure is shown in **Figure 2-6** [42]. In CuO, copper (Cu) is coordinated to 4 coplanar oxygen atoms, which lie at the corners of an almost rectangular parallelogram and the oxygen atoms are coordinated to 4 Cu atoms, which lie at the corners of a distorted tetrahedron [43]. Charge carrier (holes) concentration and typical intrinsic carrier mobility are 10^{19} cm^{-3} and 0.01 cm^2/Vs, respectively. The reason for the low mobility of charge carriers (holes) is the localization of charge carriers due to the interaction with phonons and magnons [44]. Nevertheless, CuO can be a potential candidate for PMOS because it is again thermodynamically highly stable in ambient conditions, easy to prepare by both ultra-high vacuum (UHV) and wet chemical methods, and fits into the concept of all-oxide electronics. Along with semiconducting properties, CuO has high temperature superconductivity, good magnetic (antiferromagnetic at low temperatures, < 220 K) and optical properties, which make it a suitable candidate for many applications such as magnetic storage media [42], solar cells [45], gas sensors [46], etc.

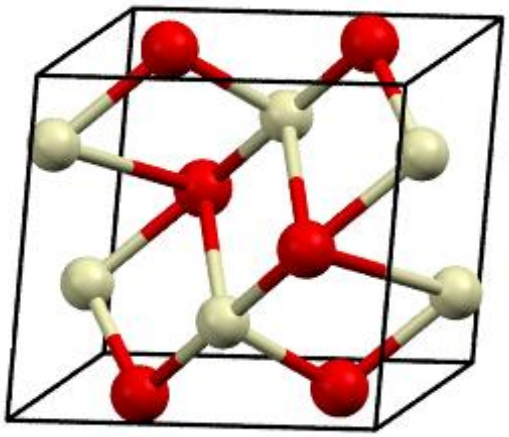

Figure 2-6 Crystal structure of CuO where copper and oxygen atoms are represented by gold and red color spheres, respectively. CuO crystallizes in the monoclinic structure [42].

Cuprous oxide (Cu_2O): Cu_2O is one of the best-known p-type oxide semiconductors because it has relatively high Hall mobility (30 cm^2/Vs) at room temperature [47]. It has a bandgap of 2.17 eV and crystallizes in the cuprite structure (**Figure 2-7**) where oxygen atoms form a body centered cubic (BCC) structure and copper atoms form a tetrahedron around each oxygen atom [48]. Other interesting features of Cu_2O are non-toxicity, high availability and it is highly used in solar cells due to high absorption coefficient. Furthermore, it can also be used in catalysis applications [49]. It can be prepared by most of the physical and chemical methods. However, it is metastable and oxidizes to the CuO phase [50].

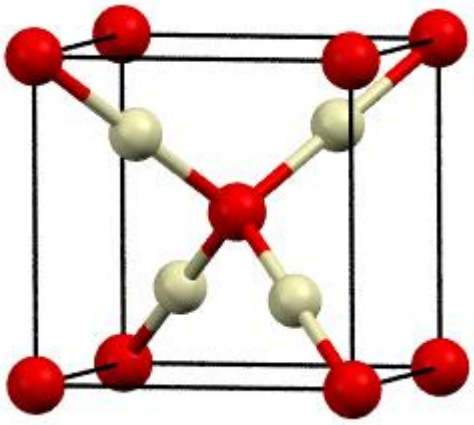

Figure 2-7 Crystal structure of Cu_2O, where copper and oxygen atoms are represented by gold and red color spheres, respectively. Cu_2O crystallizes in the body centered cubic structure [48].

2.4. Electrolyte gating

Besides semiconductors, dielectrics/insulators are also considered to be active parts of a FET device and their material and structural/morphological quality largely determine the performance of FETs. In modern technology, SiO_2 is used as a gate insulator because it naturally forms extremely smooth interfaces with Si,

which ensures high performance as insulator. However, the dielectric constant of SiO_2 is rather low (3.9), which affects the capacitance and also operation voltages. One option is to reduce the thickness of the dielectric, however, below a certain thickness limit leakage currents become too high due to tunneling of charge carriers. As a result, one option is to replace SiO_2 with another high-k insulator. However, as already has been mentioned, for solution processing/printing, both SiO_2 and other high-k dielectrics are not automatic choices because they typically require very high process temperatures to synthesize, and it is very hard or nearly impossible to prepare them with good interface quality with the semiconductor layer. In addition, their homogeneity, presence of pinholes is also another unavoidable issue, which increases leakage currents significantly. One alternative option is to use organic dielectrics, however, even in this case low dielectric constants of organic insulators results in very high operation voltage.

In this context, as a potentially suitable alternative, the possibility of electrolyte gating for printed oxide semiconductors is investigated. Within a carefully chosen potential limit, without redox-chemical reactions, electrolytes can work as ideal electronic insulator with pure ionic conductivity and no electronic conductivity. When an electrode (metallic or semiconducting) is immersed into an electrolyte, an electrical space charge region is formed at the interface. On the electrolyte side, ions of opposite charge move towards this space charge layer and form a so-called electrical double layer (EDL) at the interface (**Figure 2-8**) [51]. Initially, Helmholtz proposed the formation of this EDL and laid a good foundation for electrolytic capacitors but the assumption of constant differential capacitance is proven to be not completely true. Gouy and Chapman later proposed that the differential capacitance depends on ionic strength and applied potential. On the other hand, in the Gouy-Chapman model, the charge distribution of ions is described as a function of distance from the electrode surface but again this is not the case for highly charged double layers. Later on, Stern combined both Helmholtz and Gouy-Chapman theories and proposed a new theory, which includes that some ions are adhered to the surface (as described in the Helmholtz model) while others form a diffuse layer (as in Gouy-Chapman model). Even after 150 years of the Helmholtz model, further developments are still under way [52].

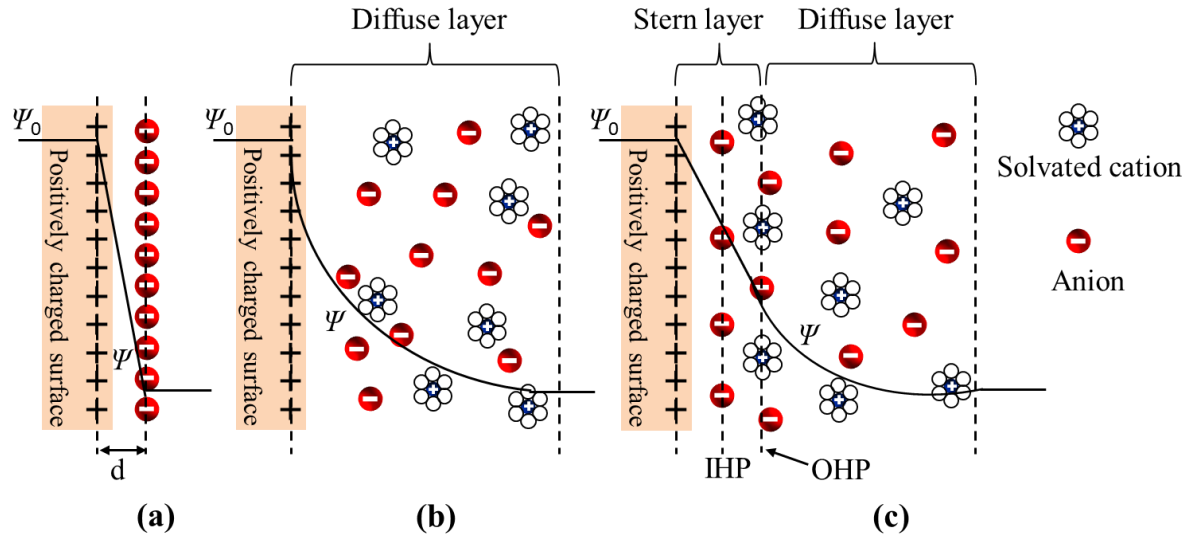

Figure 2-8 Models of the electrical double layer (EDL) at a positively charged surface: (a) the Helmholtz (b) the Gouy-Chapman and (c) the Stern model. In the figure, the inner Helmholtz plane (IHP) refers to the distance of closest approach of specifically adsorbed ions (generally anions), and the outer Helmholtz plane (OHP) refers to the non-specifically adsorbed ions (cations). The OHP is also the plane where the diffuse layer begins. d is the double layer distance described by the Helmholtz model. Ψ_0 and Ψ are the potentials at the electrode surface and the electrode/electrolyte interface, respectively [51].

The thickness of electrical double layer is rather small, i.e. about 1 nm for moderately concentrated electrolyte solutions; such a small distance (d) leads to very high capacitance ($C \propto 1/d$). This capacitance can be as high as 10 μF/cm^2 or even larger in case of pure metal electrodes. The value of this double layer capacitance also depends on the ionic strength of electrolyte. Polarization time or formation time of an electrical double layer can be as fast as 0.1 μs, which means it is in principle possible to operate the electrolyte-gated FETs in the MHz regime. Electrolytes can form very smooth and conformal interfaces with any semiconductor due to their flowability and rheological properties. On the other hand, as mentioned before, electrolytic capacitors have potential extremes for operation beyond which chemical reactions at the interface may take place. Other than this limitation, electrolytes within the critical potential can perform as gate insulator and can be a really good alternative for all-printed FETs.

Operation mechanism of electrolyte gated FETs: In case of impermeable (or electrical double layer transistor, EDLT) FETs, a carefully chosen voltage range is used for the operation of devices to avoid unwanted chemical reactions. When a voltage is applied at the gate electrode, ions of the electrolyte migrate and accumulate at the gate-electrolyte and semiconductor-electrolyte interfaces. Corresponding to the accumulation of ions, charge carriers in the semiconductor are also accumulated at the other side of the semiconductor-electrolyte interface, which results in the formation of an EDL (**Figure 2-9**). In the steady state, the gate potential significantly drops at the interface and little in the bulk of the electrolyte. Also, zero ionic current is present in the ideal case; however, that is not the case in practical applications due to the presence of impurities.

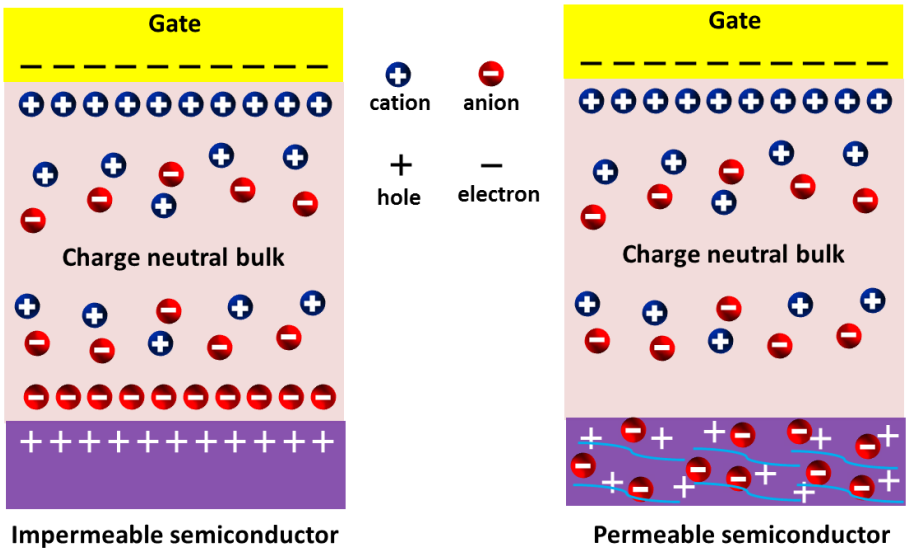

Figure 2-9 Electrolyte-gated impermeable (left) and permeable (right) semiconductor FETs. In impermeable FETs, charges do not penetrate into the semiconductor, whereas in the permeable FETs, charges penetrate into the semiconductor and cause redox reactions [53].

In case of permeable (or electrochemical transistor, ECT) FETs, ions migrate into the semiconductor and compensate the carriers, which flow from source to drain. This process is called electrochemical doping. For example, if it is a *p*-type semiconductor, anions of electrolyte migrate into the semiconductor and pair with holes of the semiconductor. However, both ions can penetrate and affect the channel conductivity, as well as morphology of the semiconductor. In this regard, EDL transistors are much better because there won't be any influence on the morphology of the semiconductor and also consistent performance is ensured [53].

Band diagrams of electrolyte gated FETs: Possible energy band diagrams of a p-type semiconductor electrolyte gated FETs are shown in **Figure 2-10**. Three different modes such as flat-band (FB), depletion and accumulation modes are shown for both EDLT and ECTs. In EDLTs, when the gate voltage (V_G) > flat-band voltage (V_{FB}), injection of electrons is inhibited due to a large energy barrier at the source-semiconductor interface (depletion mode). In accumulation mode (when $V_G < V_{FB}$), holes are injected into the valence band (or highest occupied molecular orbital, HOMO) of the semiconductor and accumulate at the interface of the semiconductor-electrolyte. In case of ECTs, a large energy level offset due to penetration of ions into the semiconductor causes depletion mode. On the other hand, in accumulation mode, holes are injected into the HOMO band of the semiconductor and cause redox reactions [53].

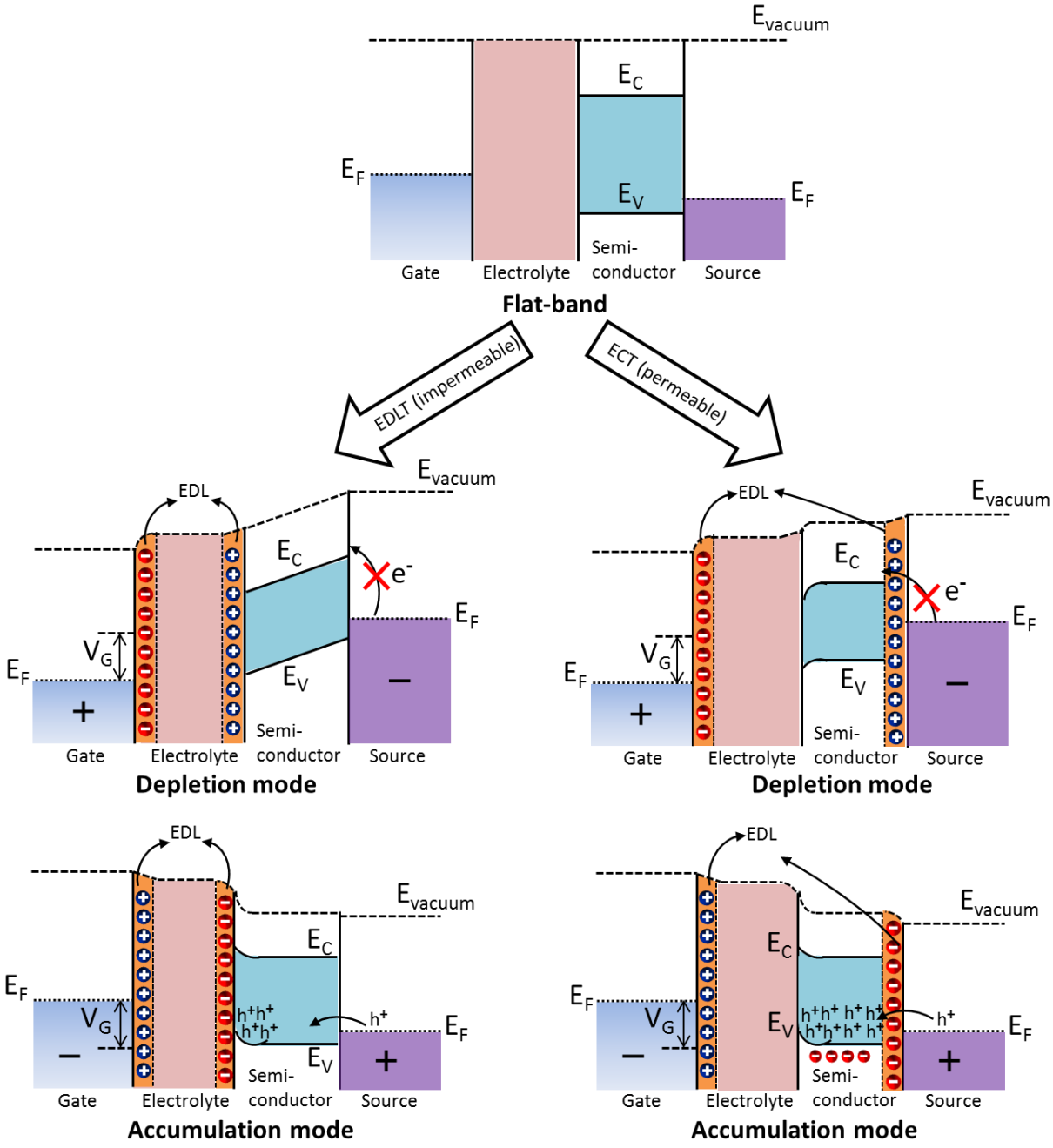

Figure 2-10 Energy band diagrams of electrolyte-gated impermeable (left) and permeable (right) semiconductor p-type FETs. Three different modes (flat band, depletion and accumulation modes) and the corresponding energy diagrams of both permeable and impermeable transistors are shown [53].

Very few groups have investigated the use of electrolytic capacitors for charge accumulation in field-effect transistor channels. Further limitations to electrolyte-gated solution-processed or oxide FETs reduce the number of investigations even more. Santos et al. have used electrolyte as gate insulator for solution processed gallium-indium-zinc-oxide (GIZO) FETs. They have prepared the electrolyte by mixing lithium perchlorate, aqueous dispersion of acrylic acid ester in styrene and aqueous dispersion of poly vinyl acetate. In their work, the achieved mobility is very low, i.e. 1 cm^2/Vs [54]. Ko et al. have reported ionic liquid-polymer gated ZnO FETs. The prepared electrolyte consists of 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide and poly-

(4-vinylphenol). Solution processed ZnO FETs showed a mobility of 3.3 cm^2/Vs [55]. Hong et al. have reported electrolyte-gated, printed ZnO FETs. They have used ion-gel, which includes a triblock polymer and ionic liquid in ethyl acetate. However, the achieved field mobility is just 1.6 cm^2/Vs [56]. Thiemann et al. prepared spin coated ZnO FETs and gated these devices with different ionic liquids. They have shown that the field effect mobility (1.9-15.9 cm^2/Vs) is varied by varying the chemical structure of ionic liquids [57]. Dasgupta et al. prepared electrolyte gated, inkjet printed In_2O_3 nanoparticulate FETs and showed a mobility of 0.8 cm^2/Vs, after processing at room temperature [58]. Many others have investigated the electrolyte for organics, two dimensional materials and also other inorganic materials such as chalcogenides, etc., [59-64].

2.5. Solution processed/printed field-effect transistors

As mentioned earlier, there is a great interest in flexible electronics in the recent times and to realize such kind of electronics, cost-effective methods such as solution processes (spin coating, printing, stamping, etc.) are used [65]. Out of many solution processing techniques, various printing methods are highly attractive for high throughput and large area fabrication of devices. The other advantages of printing methods are that these are typically inexpensive routes, and the operation is possible at ambient conditions on both plastic and rigid substrates. These additive manufacturing techniques are also attractive as extremely low-waste and high yield manufacturing route. Many researchers have explored solution processing routes to prepare FETs using organic and inorganic semiconductors (as channel materials). Although, many reports about organic FETs are present, here, only oxide semiconductors are discussed in detail. In case of crystalline semiconductors, ZnO, SnO_2 and In_2O_3 are extensively used for FETs. Among these, In_2O_3 is one of the extensively used semiconductors because of its advantages over other oxides such as high stability and high intrinsic mobility. Furthermore, it can be prepared in various forms such as films, nanoparticles, nanowires, etc. To prepare films, indium salts (indium nitrate, indium acetate, indium chloride, etc.) are dissolved in suitable solvents with or without additives and annealed at high temperatures to attain indium oxide films.

Many researchers exploited this method and prepared FETs by spin coating or printing. Kwack et al. prepared indium-zinc oxide (IZO) FETs by using electro hydrodynamic printing technique and achieved a mobility of 4.8 cm^2/Vs for the devices, which were annealed at 400 °C [66]. Wan et al. obtained a mobility of 34.5 cm^2/Vs for spin coated lithium doped IZO FETs [67]. Pecunia et al. reported solution processed IZO FETs by sol-gel on chip method. A mobility of 6 cm^2/Vs was achieved [68]. Lee et al. prepared amorphous IGZO FETs by printing and obtained a mobility of 5 cm^2/Vs [69]. Yu et al. deposited amorphous IGZO films by spray-combustion method for FETs and achieved a field effect mobility of 20 cm^2/Vs [70]. Nayak et al. reported very high mobility of 127 cm^2/Vs for spin coated and annealed (at 500 °C) In_2O_3 FETs. This high performance is due to the smooth interface between solution processed AlO_x dielectric and In_2O_3 [71]. Han et al. reported a mobility value of 55.26 cm^2/Vs for inkjet printed indium oxide transistors, where indium chloride dissolved in a

mixture of acetonitrile and ethylene glycol was used as the ink and then annealed at 500 °C [72]. Kim et al. used a novel combustion route (nitrate salt with added fuel to reduce the decomposition temperature) to prepare oxide FETs and for In_2O_3 (annealing temperature was 325 °C), the mobility was 9.4 cm^2/Vs [73]. Kim et al. prepared In_2O_3 FETs by annealing (at 400 °C) the spin coated $InCl_3$, which is dissolved in 2-methoxyethanol (with ethanolamine) and the achieved mobility was 44 cm^2/Vs [74]. On the other hand, completely room temperature processed FETs using indium oxide nanoparticles are also reported by Dasgupta et al. with an achieved mobility of 0.8 cm^2/Vs [58].

In the case of p-type oxides, CuO and Cu_2O can be the material of choice due to ease of preparation, high stability in ambient conditions, and relatively good electronic performance among other available alternatives. These two oxides can be prepared in different morphologies such as nanoparticles, nanowires, nanorods, etc. Many researchers have reported solution processed PMOS FETs using either of these oxides. Yu et al. reported Cu_xO FETs by spin coating copper acetate films and vacuum annealing at 600 °C to obtain a mobility of 0.29 cm^2/Vs [75]. Pattanasattayavong et al. reported spray deposited Cu_2O FETs and the achieved mobility was 0.01 cm^2/Vs [76]. Kim et al. prepared Cu_xO FETs by spin coating Cu acetate films, which are annealed at 700 °C in a controlled atmosphere and achieved a field effect mobility of 0.16 cm^2/Vs [77]. However, in general it may be noted that the number of reports on solution processed PMOS are less and the achieved mobility values or performances are far less than the NMOS counterparts. However, putting it into a positive outlook, this also means that there is quite some scope to improve the oxide PMOS devices towards all-oxide printed/flexible electronics.

2.6. Inkjet printing

It is important to use suitable techniques or methods to realize cost effective, large area, flexible electronics. Although many inexpensive solution based methods such as spin coating, doctor blading, spray coating etc. have been extensively used, the printing method is the one that can be best suited for flexible electronics due to the large range of advantages it offers such as high throughput, roll-to-roll manufacturing, non-vacuum, mask-less, and non-contact processability (eliminating the contamination problem [62]), etc. Printing means transferring the desired material on suitable substrates, and in case of printed electronics, electronically functional materials are used as ink and deposited on a suitable substrate to achieve required circuits.

Several printing techniques such as gravure, offset, flexography, screen, pad, digital and inkjet printing can be used to provide functional electronic patterns based on the need/demand of the specific application. Out of these techniques, inkjet printing is always favored at research facilities owing to its digital nature and large range of versatilities it offers. Inkjet printing can produce high resolution patterns. It is a non-contact method, which therefore eliminates contamination issues. Furthermore, a wide range of inks with varied fluid dynamic properties can be used. In the inkjet method, three categories are present based on the way droplets are generated, i.e. thermal (explosion of ink due to heating element), piezoelectric (electronic pulse creates

mechanical pressure) and continuous (constant pressure is applied) [78]. Most of the modern day printers are based on piezoelectric transducers due to better control over the drop formation, reliability and no harm to other parts, etc. The operating principle is that the voltage applied to piezoelectric actuator causes sudden change in the volume, which creates pressure waves, which propagates throughout the capillary. The positive pressure wave approaches the nozzle and the fluid is pushed outwards. The droplet is ejected when the kinetic energy transferred is more than the surface energy, which is needed to form a droplet. The schematic of a nozzle is shown in **Figure 2-11**.

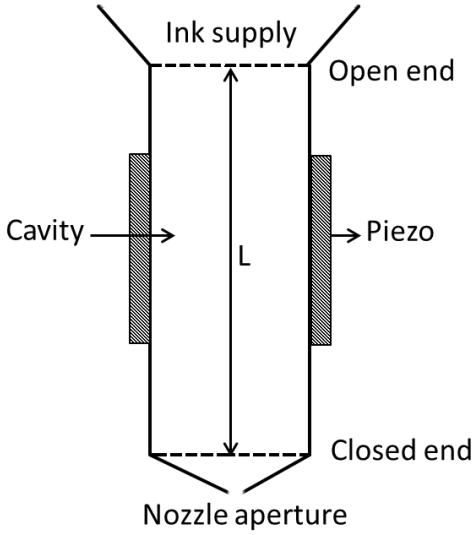

Figure 2-11 Schematic of an inkjet printer nozzle. It shows the ink supply, cavity for the ink, piezoelectric transducer (creates pressure pulses) and nozzle aperture (to release the ink) [79].

The successful droplet ejection depends on the fluid properties of ink (surface tension and viscosity) and instrumental parameters (voltage, pulse width, length of fluid cavity, frequency, etc.). Fromm et al. have calculated a dimensionless number z, which is the inverse of Ohnesorge number (Oh). The value of this inverse Ohnesorge number (Oh^{-1}) describes easy printability of the inks and is given by:

$$z = (l\rho\gamma)^{1/2}/\eta = (Oh)^{1/2} \qquad (2.7)$$

where l=characteristic length (diameter of nozzle aperture), ρ =density, γ = surface tension, η = viscosity. Fromm predicted that drop formation is possible when $z > 2$ and Derby et al. found that $1 < z < 10$ also works for printing and further studies on droplet ejection are going on [79]. The next important thing is film formation, which is highly influenced by substrate's surface energy; however, impact of the fluid can't be neglected. Often, the printed droplets exhibit a coffee ring effect in which solute try to deposit at the boundary, which causes a thick edge and thin inner features. The reason for this is given by pinning of the droplet edges and capillary flow from the center to the edges as the evaporation continues. The addition of a second solvent with a higher boiling point creates a surface tension gradient and changes the evaporation rate, which in turn reduces the flow of solute outwards, thereby reduces the coffee ring effect significantly [79]. Yunker et al. reported that the coffee

ring effect can be eliminated by using ellipsoidal particles, which have strong capillary interactions, which prevent them to reach edges and confirms uniform deposition [80].

2.7. Oxide nanoparticle dispersion versus oxide precursor routes for printed oxide transistors

Solution processed oxide FETs can be prepared using nanoparticles or chemical precursors. In the nanoparticle route, pure nanoparticles with a suitable size (20-50 nm for inkjet printer, which has a typical nozzle diameter of 20 μm) are dispersed in a suitable solvent stabilized either by electrostatic, steric or electrosteric stabilization. In electrostatic stabilization, nanoparticles have common surface charge, whereas in steric stabilization polymer additives, which adsorb on the surface, act as protective agents. On the other hand, electrosteric stabilization is achieved by the combination of adsorbed polymer or polyelectrolytes and electrical double layer repulsion [81]. The major benefit of dispersed inks is that they can be printed at room temperature (RT) to realize flexible electronics on any inexpensive substrate of choice. This route is suitable for almost all kinds of materials such as metals, semiconductors, and also dielectrics. However, films produced from these inks usually show porosity, lack of good interparticle contact, and sometimes even cracks in the printed layer; all these things hinder the electrical transport and thereby lower the performance [58].

In the precursor route, metal salts (nitrates, acetates, chlorides etc.) are dissolved in suitable solvents and used as inks to prepare functional circuits. These precursor based inks typically require an annealing step in order to convert them into the oxide semiconductor phase of choice. Precursor derived printed layers typically result in good quality films in comparison with nanoparticulate films. Therefore, usually superior electrical performance is achieved, however, at the price of the requirement of the additional annealing step [82]. To reduce the decomposition temperature of precursors, novel techniques such as sol-gel on chip [83], combustion synthesis [73], photonic curing [84] etc. have been proposed. These approaches show partial success. However, the temperatures are still not low enough to be compatible with the inexpensive polymer substrates such as polyethylene terephthalate (PET).

2.8. Characterization techniques

In the present work, different characterization techniques have been used to analyze the phases, the morphology, the roughness, the interfacial structure, the chemical composition, the capacitance, the electrical characteristics, etc. In this section, an overview of X-ray diffraction (XRD), scanning electron microscopy (SEM), atomic force microscopy (AFM), transmission electron microscopy (TEM), X-ray photoelectron spectroscopy (XPS), impedance spectroscopy (IS), cyclic voltammetry (CV), etc., is presented.

2.8.1. X-ray diffraction

X-rays (discovered by Röntgen in 1895) are electromagnetic radiation with wavelengths in the range of 0.01-10 nm [85]. X-rays are produced by decelerating charge carriers (electrons) of sufficiently high kinetic energy. This method generates characteristic lines (sharp intensity maxima at well determined wavelengths), which are superimposed on the continuous spectrum. The characteristic lines can be referred to the electron shells K, L, M, etc., in the order of increasing wavelength. Out of these, in general, characteristic lines of K are useful for diffraction, because longer wavelengths can be easily absorbed. For example, the K lines of a molybdenum (Mo) target have a wavelength of about 0.7 Å and are used for diffraction experiments. The diffraction is a scattering phenomenon, in which scattered waves (x-rays) form constructive interference (reinforcement of two or more waves) at certain angles. W.H. Bragg and W.L. Bragg proposed a condition for diffraction, called as Bragg's law:

$$n\lambda = 2d\ sin\theta \qquad (2.8)$$

where λ is wavelength, d is distance between atomic planes, θ is Bragg angle and n is an integer other than zero.

X-ray diffraction technique is non-destructive and useful to find out the crystal structure, grain size, phase, lattice parameters, interatomic distances, etc. of powders as well as thin films. However, safety precautions are necessary while handling the instrument due to harmful radiation [86].

2.8.2. Scanning electron microscopy

In the SEM, a fine beam of accelerated electrons interact with the sample while scanning the surface and produce various signals that contain information such as topography, composition, etc. The interaction of an electron beam with the sample can be divided into two major categories, i.e. elastic and inelastic scattering. In elastic scattering, the electrons incident on a specimen deflect either by nuclei or outer shell electrons (of atoms of specimen) of similar energy. This scattering is characterized by negligible energy loss and the electrons that are scattered by more than 90° angle are termed back scattered electrons (BSE). The intensity of BSE signal depends on the atomic number, i.e. elements with higher atomic number results in a better signal compared to lower atomic number elements. Therefore, the BSE signal can be used to analyze both morphology and composition. However, the lateral resolution of BSE (1 μm) is not as good as that of secondary electrons (SE) (10 nm), because the BSE signal is generated from a larger region than that the signal of the SEs. On the other hand, in inelastic scattering, the incident electrons lose energy upon interacting with the atoms of specimen. In this scattering process, SEs are generated during ionization of specimen atoms. SEs have less energy (< 50 eV) and consequently can only escape from a depth of only a few nanometers below the sample surface. Hence, SEs are mainly useful to analyze the surface morphology of the samples. In addition to the BSE and the SE signals, characteristic X-rays, auger electrons and cathode-luminescence signals, etc., are also produced during the interaction of electron beam with the specimen. Characteristic X-rays and auger electrons provide chemical

composition and chemical information (for example composition maps) of the investigated samples, respectively [87-89].

A typical SEM instrument has different parts such as electron gun (generates the electron beam), condenser lens (to adjust the diameter of the electron beam), objective lens (to focus the beam), detectors (to detect SE and BSEs), and display unit (to display the image) [89]. Using the SEM all kinds of samples including metals, semiconductors, ceramics, biological substances, etc., can be analyzed. However, non-conducting samples (in case of conventional SEM) need a conducting coating (e.g., few nm of gold or carbon) to avoid charging effects. Most of the SEM instruments operate in high vacuum to avoid any deflection of the electron beam.

2.8.3. Transmission electron microscopy

In a TEM, a very thin sample (< 100 nm) is irradiated with a high energy electron beam. The incident electron beam interacts (by elastic or inelastic scattering) with the sample and is transmitted through the entire sample thickness [90]. This transmitted beam carries the information (crystal structure, defects, composition, morphology, etc.) of the sample and is used to obtain a bright field image. In the bright field imaging mode, thicker regions or higher atomic number elements appear as dark (due to higher scattering of the electrons) and very thin regions appear as bright areas. This mode reveals the nature of the sample (morphology, defects, etc.) and is the most commonly used mode. In addition to the transmitted beam, diffraction of electrons occurs during the interaction of electrons with the atoms in the sample, leads to dark field images. In this mode, regions without any sample appear dark and diffracted areas appear bright. Defects such as stacking faults, planar defects, etc., can be revealed in this mode. Furthermore, diffraction patterns (DP) can also be obtained by adjusting the magnetic lenses, i.e. back focal plane of the lenses (instead of imaging plane) is placed on the imaging apparatus. DPs reveal the information related to the crystal structure of the sample. On the other hand, energy dispersive spectroscopy (EDS) can be used to find out the elemental composition of the samples. In EDS, characteristic X-rays, which are specific to an element, are measured. Another mode of TEM is electron energy loss spectroscopy (EELS), in which energy loss of scattered (inelastic) electrons due to the interaction with the atoms of the sample is measured. EELS can be used to analyze composition, bonding, surface properties, etc., and it is highly useful for lower atomic number elements due to sharp excitation edges, measureable energy losses, etc. [91].

The major advantage of TEM compared to SEM is the much higher spatial resolution. In the best and most modern TEMs, a resolution in the order of 0.5 Å has been obtained. Therefore, it is possible using TEM to observe atoms, defects, etc. However, very thin samples (<100 nm) have to be prepared for TEM analysis. Thin samples can be prepared by electro-polishing (dissolution of materials using electrochemical reactions) or focused ion beam (high energy ions are used to mill the sample) techniques.

2.8.4. Atomic force microscopy

In an AFM, a cantilever with a sharp tip or probe (made of silicon, silicon nitride, etc.) scans the surface of the sample. The force between the tip and the sample deflects the cantilever according to Hooke's law (within the elastic limit, force ∝ distance). The deflection of the cantilever is measured by a laser beam deflection optical detection system. Based on the tip and sample interactions, AFM can be operated in three different imaging modes, i.e. contact, non-contact and tapping modes. In contact mode, the tip of cantilever is in direct contact with the sample's surface. In this mode, the tip operates in the repulsive force regime (according to force vs distance curve) and the deflection of cantilever is kept constant by the feedback loop (controls the height of the tip). The image contrast depends on the applied force, which depends on the spring constant of the cantilever. This mode is extensively used due to the high resolution and the better scan speeds compared to other modes. However, this mode is also sensitive to the nature of the sample and there is a possibility of damaging either sample or tip due to the direct contact. In the non-contact mode, a tip oscillating with its resonance frequency is brought close to the sample's surface and the frequency shift due to the van der Waals attractive force is measured. To take images, a constant frequency shift is maintained by feeding the amplitude value at a fixed frequency to the feedback loop. In this mode, the tip-sample interactions are small and a good vertical resolution can be obtained. However, lateral resolution is lower than in other modes and this mode can't be operated in a liquid medium. On the other hand, the principle of tapping (intermittent contact) mode is similar to non-contact mode, except the tip is brought into contact during oscillation. The dampening of the cantilever oscillation amplitude is caused by the repulsive forces, which are also present in the contact mode. The oscillation amplitude of the cantilever in the tapping mode is more than the non-contact mode. Vertical as well as lateral resolutions are good in this mode and also tip-sample interactions are less compared to the contact mode. Tapping mode can also be used in liquids [92, 93].

Not only two-dimensional but also three-dimensional images can be obtained by AFM. However, AFM is not useful for scanning large areas (> 100 μm) due to the limitation in scanning speeds. AFM can be used for conducting, non-conducting, biological samples, etc. and also in different environments.

2.8.5. X-ray photoelectron spectroscopy

In the XPS, the sample is irradiated with mono-energetic X-rays (Al Kα (1486.6 eV) or Mg Kα (1253.6 eV)) and the energy of the emitted electrons is analyzed. The incident photons interact by the photoelectric effect and cause the emission of electrons originating from the atoms at the surface. The kinetic energy (KE) of the emitted electrons is:

$$KE = h\upsilon - BE - \Phi s \qquad (2.9)$$

where, hυ is energy of the incident photon, BE is binding energy, Φs is spectrometer work function. The binding energy is the ionization energy of the atom for the particular shell involved [94]. BE is unique to each and every electron of a particular shell of the atom. The spectral lines of XPS are identified to the shell from which the

electrons are emitted (1s, 2s, 2p, etc.) In the XPS, it is possible to identify almost all the elements of the periodic table except hydrogen and helium. XPS is useful for analyzing the valence state of elements and compositions of the samples as well. However, XPS is surface sensitive, i.e., it can detect the elements, which are in the top layers close to the surface (≤ 10 nm) only. This is due to fact that only the electrons from a few atomic layers beneath the surface can escape without any energy loss, and these electrons can be detected for the analysis [95].

2.8.6. Impedance spectroscopy

In the IS, the impedance (Z) of an electrochemical cell can be measured by applying a voltage or a current at a particular frequency and measuring the phase shift as well as the amplitude (or real and imaginary parts) of the resultant current at that frequency using analog circuit or fast Fourier transform analysis. The parameters measured by IS can be divided into two categories: the first one is related to the material, i.e., conductivity, dielectric constant, mobility of charge carriers, equilibrium concentration of charged species, etc. The second one is related to the electrode-material interfaces that include adsorption-reaction rate constants, capacitance of the interfacial region and also diffusion coefficient of neutral species [96].

The impedance can be represented by two different plots, Nyquist and Bode plots. In a Nyquist plot, the real part of the impedance (Z') is plotted versus the imaginary part (Z''). The plot is in a semicircle shape and each point on it (semicircle) represents the impedance at a particular frequency. However, the exact value of this frequency is not known. This is one of the limitations of the Nyquist plot. On the other hand, in a Bode plot, the impedance magnitude and the phase angles are plotted as a function of frequency. The frequency values are known in the Bode plot. However, the estimation of the characteristic frequencies in complicated electrochemical systems that involve additional impedance components is difficult in the Bode plots as well [97].

IS is a powerful tool to study the kinetics at electrode-electrolyte interfaces, the conduction mechanisms in the materials, the electrical properties such as impedance, capacitance, inductance, etc., and has been shown to be useful for corrosion studies. IS has been extensively used in different fields such as energy-storage systems, biological analysis, biomedical sensors, etc. [96, 97].

2.8.7. Cyclic voltammetry

CV is an electrochemical method, in which a cyclic potential (*E*) with a certain scan rate (V/s) is applied to the electrode while the current (*I*) response is measured. The analysis of the current gives information about the thermodynamics as well as kinetics of the reaction at the electrode-electrolyte interface. For CV measurements, a three electrode system (working (WE), reference (RE), counter (CE) or auxiliary (AE) electrodes) is used, in which the potential is applied between WE and RE, while the current is measured between WE and CE. The material to be characterized and the silver / silver chloride (Ag/AgCl) electrode are used as WE and RE, respectively. The choice of CE depends on the WE and it mainly balances the redox reactions by an electron

transfer of opposite direction, i.e., if oxidation takes place at WE, reductions takes place at CE [98]. However, for low currents and high conducting electrolyte solutions, a two-electrode (WE and CE) cell is sufficient for CV measurements [99].

By using CV measurements, the double layer capacitance at the electrode-electrolyte interface can be determined, and it is the ratio of current and scan rate. The specific capacitance can be obtained by dividing the capacitance with the area of the electrode. Furthermore, CV measurements can also be used to study the reaction mechanisms of organic, organometallic, inorganic, and also pharmacological chemistry [98].

3. High Temperature Annealed Oxide Transistors

The crystallinity and the film quality play a major role in determining the performance of crystalline oxide semiconductors. Precursors can provide crystalline films of good quality after a high temperature heating step. Here, an attempt is made towards developing high performance oxide transistors and CMOS logics by combining films prepared by the precursor route with highly efficient gate dielectric (electrolyte). This chapter presents the preparation and characterization of oxide FETs and CMOS logics.

3.1. Printed oxide transistors using precursors annealed at different temperatures

In this section, indium oxide FETs are prepared using indium chloride as the precursor and an electrolyte as the gate insulator. Two different heating rates are used to investigate the effect of crystallite size on the performance of FETs.

3.1.1. Preparation of precursor-route transistors

The concentration of the precursors plays a role in determining the performance of the transistors. For example, very low concentration causes insufficient percolation but too high a concentration leads to high conducting films (in this case, the transistor would be difficult to switch off). The optimization process showed that 0.05 M of indium salt has been found to be the optimum concentration, and consequently, this concentration has been used in the following studies. Indium oxide precursors were prepared by dissolving 0.05 M indium chloride tetrahydrate ($InCl_3 \cdot 4H_2O$) in water and ethanol (volume ratio of 1:1) and after thorough mixing, the solution was filtered through a 0.2 μm polyvinylidene fluoride (PVDF) membrane filter. The filtration removes big size impurities and undissolved salts present, thus, avoiding clogging of the print head nozzles. The filtered solution was used directly as the ink to print the channel of the FETs on the glass substrate that had been already lithographically patterned to provide indium tin oxide (ITO) passive structures (source (S), drain (D), and gate (G) electrodes). The reason to choose ITO as electrode material is that it is very stable with the electrolyte (no chemical reactions within the potential window of 1 V) [100] and has similar or lower work function (3.9-4.2 eV) compared to indium oxide (4.3-4.5 eV) [101]. For n-type semiconductors, electrodes with similar or lower work function result in an Ohmic contact, i.e., no barrier for the flow of electrons [18]. Next, the devices were prepared with in-plane FET geometry. Therefore, all the passive elements (metal electrodes) can be patterned using a single lithography step and they are placed on the same plane (**Figure 3-1**)

of the substrate. The channel length (*L*) has been fixed at 50 µm. While for Si-based FETs, either bottom or top gate configurations have been used, in the present case, an in-plane design is favorable because the electrolyte used as the gate insulator cannot be exposed to ultra-high vacuum for the deposition of electrodes as needed in bottom- and top-gate geometries. The reason is that the trapped solvent molecules of the electrolyte would evaporate during vacuum processing, and will lead to low ionic conductivity of electrolyte.

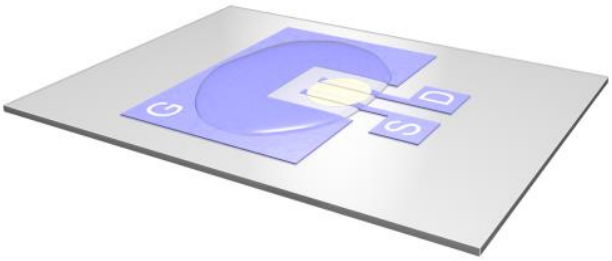

Figure 3-1 Schematic of an in-plane transistor. It shows gate (G), source (S), drain (D) electrodes with printed channel and electrolyte.

Prior to printing, the glass substrates were cleaned with isopropanol and dried by purging with dry nitrogen. The indium oxide precursor was printed on this cleaned and pre-patterned substrate. To print the precursor, a voltage of 40 V (at piezo), meniscus set point of 0.5, drop spacing of 20 µm and standard Dimatix waveforms are used. The printed precursors have been dried at 100 °C for 2-3 minutes followed by immediate transfer to a muffle furnace. During the drying process the solvent evaporates and forms a film consisting of the indium salt, which decomposes to indium oxide at high temperatures. Therefore, the dried films were annealed at different temperatures (300-500 °C) with a heating and cooling rate of 1 °C/min. After annealing of the printed channels, optical images were taken to calculate the width (*W*) of the channel, accurately. In parallel, the printable electrolyte solution was prepared by mixing two separately prepared equal amounts of aqueous polyvinyl alcohol (PVA, with a molecular weight of 13000-23000 g/mol, prepared at 75 °C) and aqueous potassium fluoride (KF) solution (both using de-ionized water with more than 18.2 MΩ-cm electrical resistivity). The mixture was then completely homogenized by continuous stirring for more than 12 h. The prepared polymer electrolyte was filtered through 0.45 and 0.2 µm PVDF membrane filters in series. The prepared electrolyte mixture is then ready to be printed on the annealed channels of the printed FETs. The printed CSPE solution was allowed to dry at room temperature with evaporation of excess solvent. Next, the prepared indium oxide FETs were characterized at ambient conditions using Agilent 4156C semiconductor parameter analyzer and Süss microtec EP6 probe station.

3.1.2. Structural and Electrical Characterization

For the structural characterization, a similar batch (same as device substrates) of glass substrates were used to print and anneal the precursor solution following identical printing and annealing conditions. X-ray diffraction (XRD) measurements were performed using Philips X-ray diffractometer with Cu-Kα radiation where the working current and voltages are set to 40 mA and 45 kV, respectively. The XRD patterns (**Figure 3-2**) show that the spurious second phase indium oxychloride (InOCl) exist along with desired In_2O_3 for the

precursor that is annealed at 300 °C, as a result of the incomplete decomposition of the precursor. Rietveld refinements (**Figure 3-3**) using Fullprof software with Pseudo-Voigt method were performed for these patterns and it was found that approximately 8% of InOCl is present. InOCl is an insulating phase and detrimental to the electronic transport. The effect of InOCl is clearly evident in the electrical characterization of these films, which will be discussed in the following sections. On the other hand, pure In_2O_3 (ICSD No. 06-0416) was obtained for the 400 and 500 °C annealed samples. The conclusion from the XRD patterns is that the indium chloride forms InOCl after dissolving in the solvents, which decomposes to indium oxide at high temperatures. Furthermore, it is important to know the crystallite size of these samples because it can assist in understanding the grain boundary scattering phenomenon of electrons and thereby field-effect mobility of the devices. The calculated crystallite sizes vary with annealing temperature (**Table 3-1**). The table indicates that the prepared films have relatively large crystallites (86-101 nm), which is due to the extreme slow heating and cooling conditions (1 °C/min). These slow heating conditions provide sufficient time for the decomposition of salts and also growth of nucleated crystals. It is observed that the crystallite size generally increases with temperature, but for the 500 °C annealed sample the crystallite size is found to be lower than 400 °C. The reason may be due to the fact that at high annealing temperatures, which is more than the strain point (490 °C) of the glass substrate [102], may have caused significant roughness and irregularities in the glass substrate. It may have led to additional heterogeneous nucleation of the oxide phase during the first phase of annealing, thereby decreasing the crystallite size. Here, the values of crystallite size are calculated using Debye-Scherrer equation [103]:

$$d = \frac{0.9\,\lambda}{\beta \cos\theta} \qquad (3.1)$$

where, d, λ, θ and β are the volume average of crystallite size, the wavelength of the radiation in Angstrom (Å), the diffraction peak position in radian, and full width at half maxima, respectively.

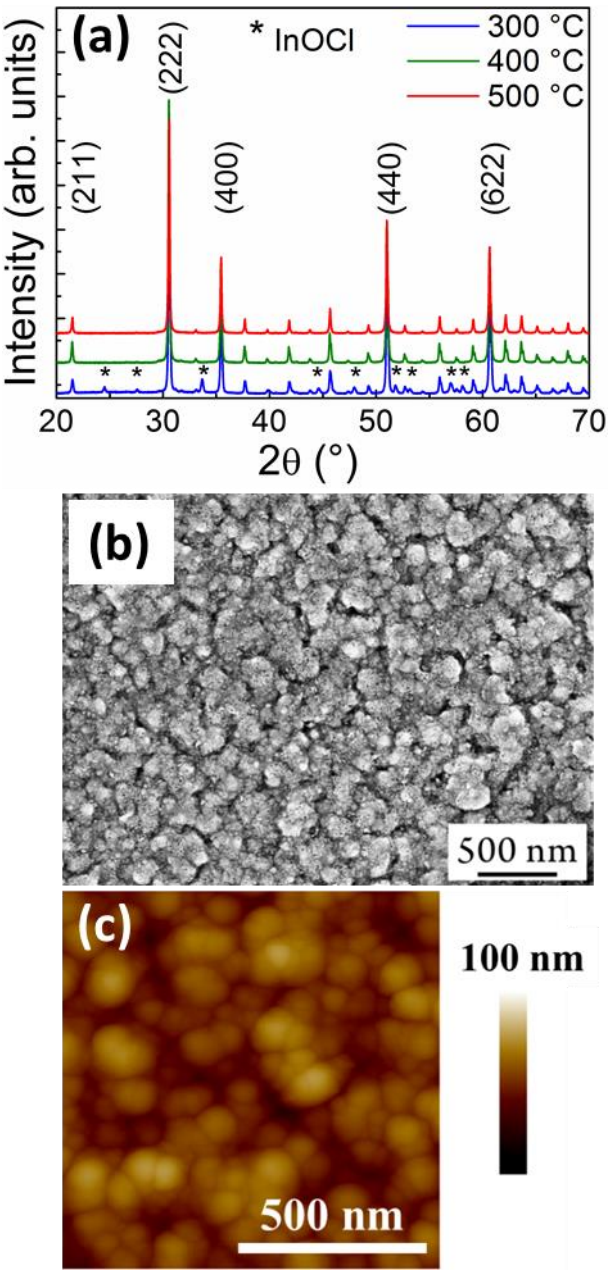

Figure 3-2 (a) XRD patterns of samples prepared from indium oxide precursors, which are annealed at different temperatures and (b) SEM, (C) AFM images of 400 °C annealed sample. XRD patterns are indexed with Miller indices (atomic planes) of standard indium oxide phase and star mark symbol shows the reflexes of InOCl phase.

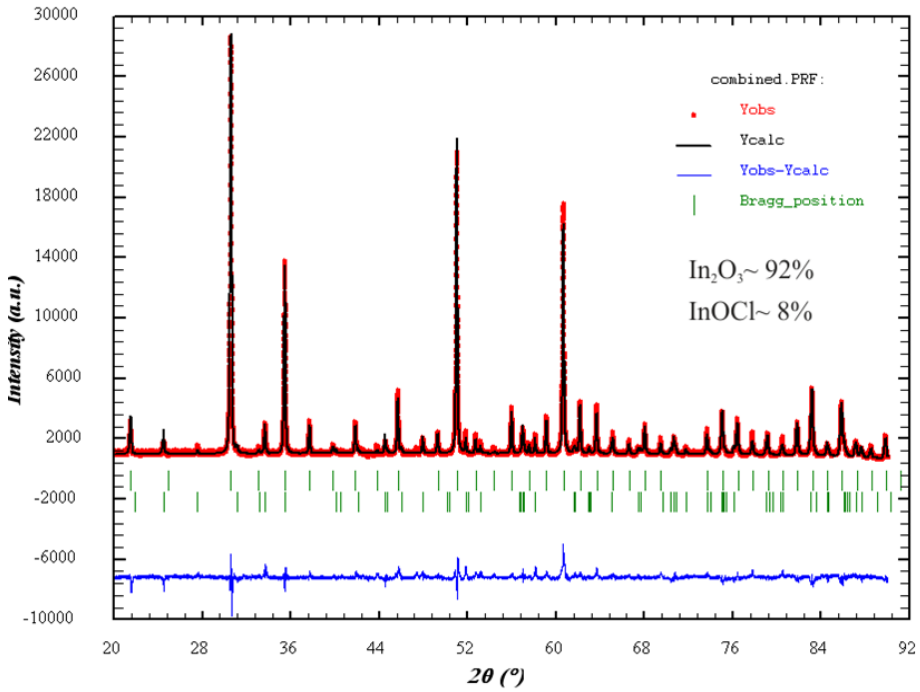

Figure 3-3 Rietveld refinement of the XRD pattern of indium oxide precursor after heat treatment at 300 °C. It indicates the percentages of indium oxide (92%) and indium oxychloride (8%).

Temperature (°C)	Crystallite size (nm)	
	In_2O_3	InOCl
300	86	53
400	101	-
500	95	-

Table 3-1 Crystallite sizes of indium oxide precursors which are annealed at different temperatures (300-500 °C). InOCl is present in samples annealed at 300 °C, however not in samples annealed at 400 °C and 500 °C.

To characterize the morphology of the printed In_2O_3 layer, scanning electron microscopy (SEM, Zeiss Leo 1530) and atomic force microscopy (AFM, Bruker dimension icon) have been used. SEM images of 400 °C (**Figure 3-2b**) annealed samples clearly show a solid network of particles with no observable porosity. The AFM image (**Figure 3-2c**) of the same sample shows a very identical interparticle network; the particle size that is observed for both the techniques, nearly matches to the XRD crystallite size and the roughness is found to be around 8.3 nm. The SEM and AFM images of the 300 °C and 500 °C annealed samples (**Figure 3-4 a-d**) also agree with the particle size that is calculated from XRD. The film quality in these cases is also found similarly good: root mean square (R_{rms}) roughness values are found to be 8.5 and 3.5 nm, respectively. Surface roughness analysis of all three samples is shown in **Figure 3-5**. The analysis of the surface roughness indicates that the films have little high roughness (> 3 nm). The reason for a little high roughness value is the use of water as a solvent, which dries slowly. It has also been reported earlier that halide salts tend to produce films with higher surface roughness [104]. However, surface roughness is of less importance in electrolyte gating due to the

flowability of electrolyte on any surface profile. Electrolyte can provide a smooth interface even for rough indium oxide films which is evident in the cross-section image (**Figure 3-6**). Furthermore, the section analysis of AFM micrographs (**Figure 3-7**) shows that the precursor-derived In_2O_3 thin film that has been annealed at 400 °C has bigger particles compared to other two annealing temperatures. It has been later realized that particle size also plays a crucial role in determining the field-effect mobility values due to strong impact of grain boundary scattering at smaller particle sizes. Therefore, from the present study, it can be concluded that the optimum temperature in order to obtain smooth as well as single phase indium oxide films would be 400 °C.

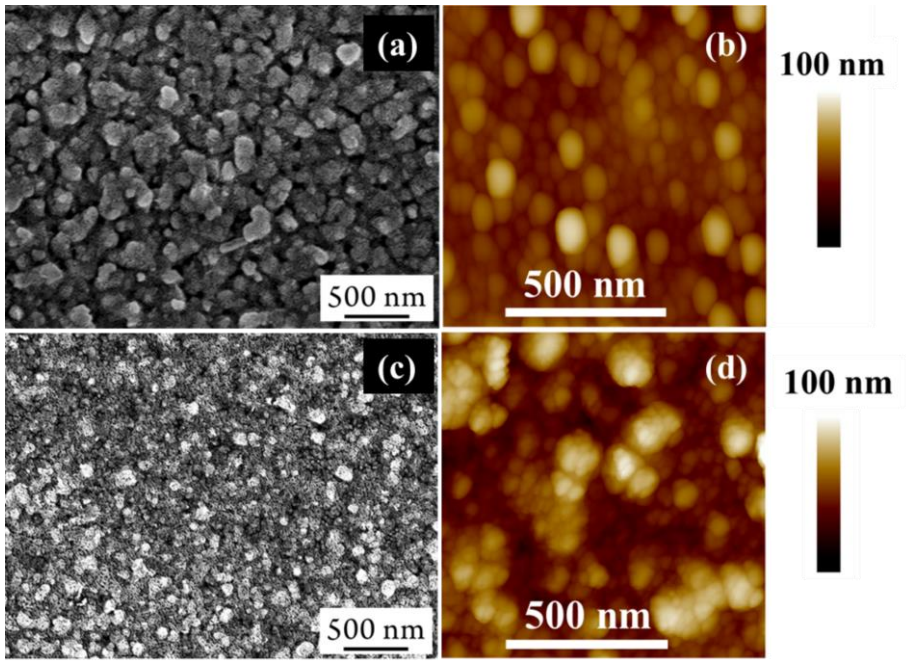

Figure 3-4 SEM and AFM images of precursors after annealing at 300 °C (a & b) and 500 °C (c & d) SEM and AFM images of precursors which are annealed at 300 °C (a & b) and 500 °C (c & d)

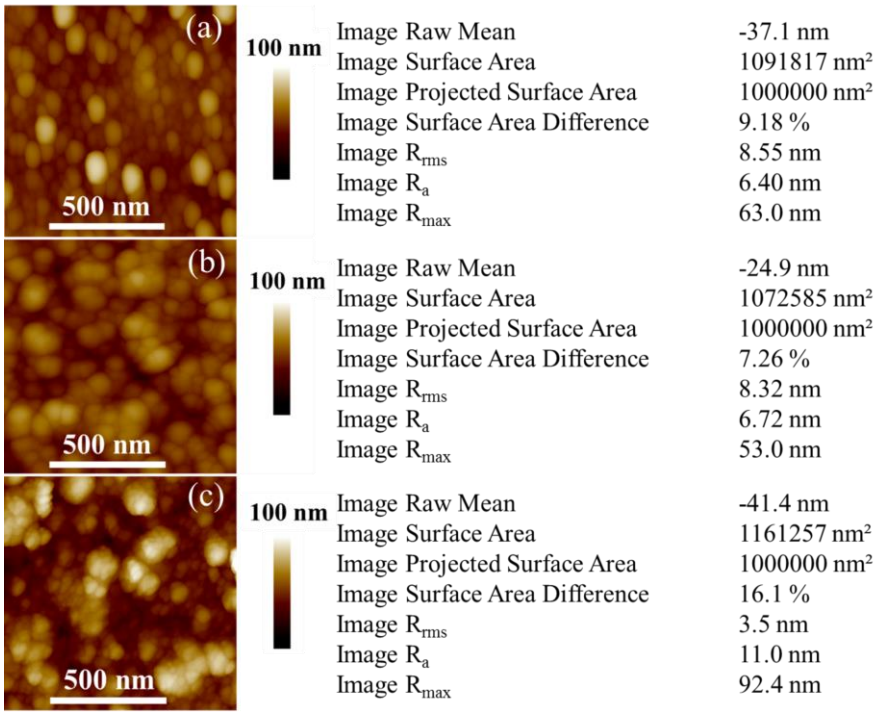

Figure 3-5 Surface roughness analysis (right side) of AFM micrographs (left side) of precursors after annealing at (a) 300 °C (b) 400 °C and (c) 500 °C, respectively. Roughness analysis has been carried out by nanoscope analysis software from Bruker dimension icon AFM. In the roughness analysis, image raw mean is the mean value of image data without application of plane fitting, image surface area is the three-dimensional (3D) area of the image, image projected surface area is the area of the image rectangle, image surface area difference is the difference between the image's 3D surface area and the projected surface area, R_{rms} is the root mean square average of height deviations taken from the mean data plane, R_a is average roughness, R_{max} is the maximum vertical distance between the highest and lowest data points in the image [105].

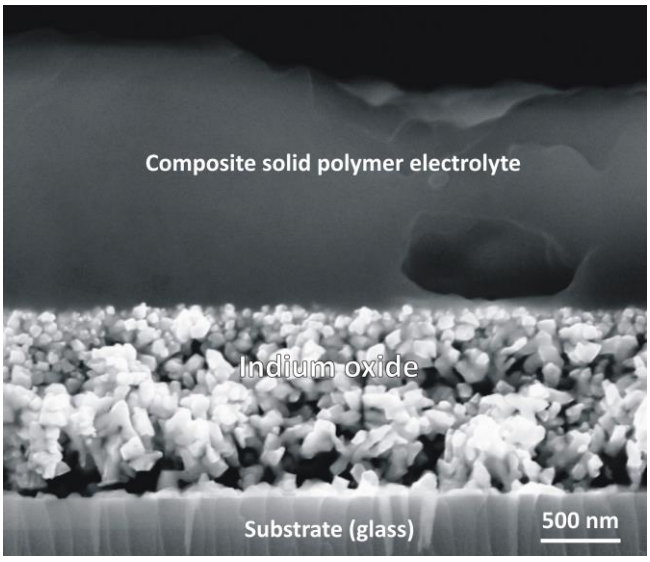

Figure 3-6 Cross-section SEM image showing the interface between indium oxide and composite solid polymer electrolyte.

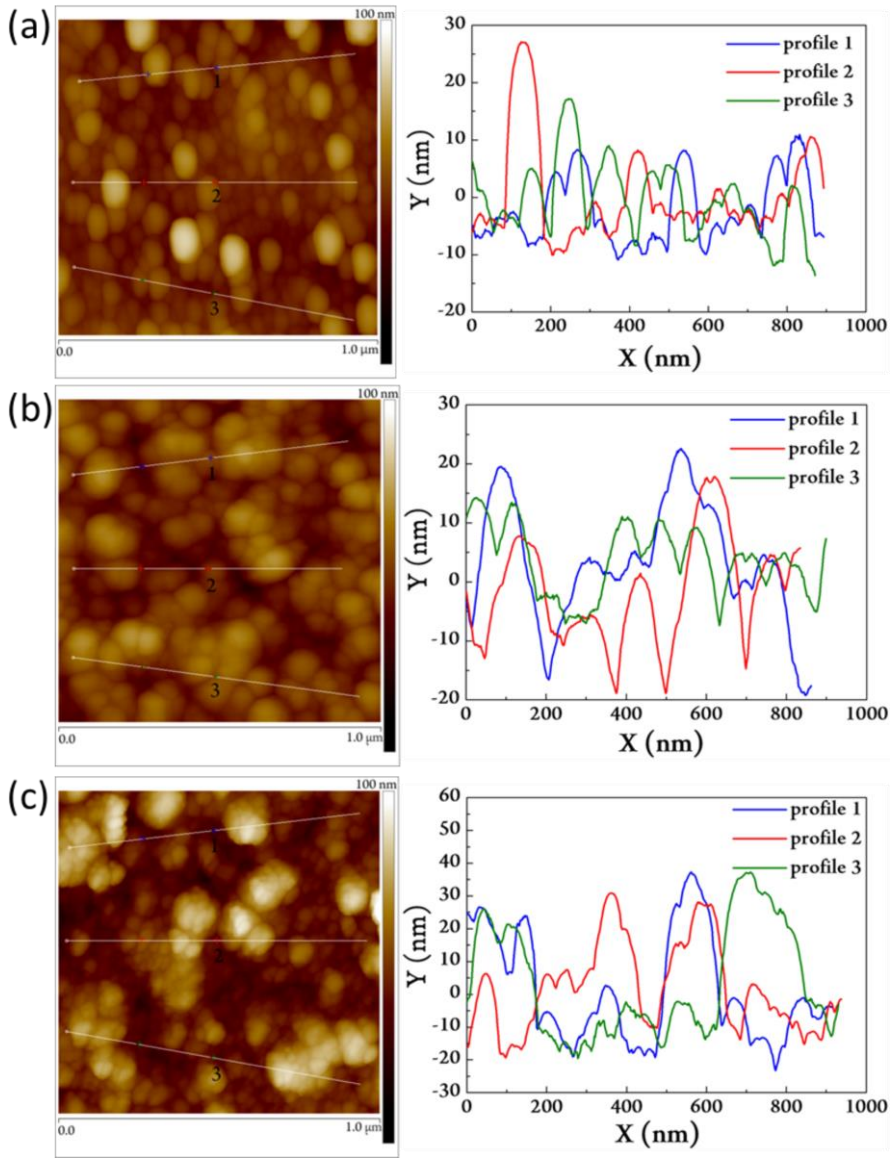

Figure 3-7 Section analysis of AFM micrographs of precursors after annealing at (a) 300 °C (b) 400 °C and (c) 500 °C, respectively. Line profiles show the distribution of different particles of the indium oxide precursor films.

Electrical characterization of all the FETs was performed in air and at room temperature. To measure the transfer curves, constant voltage (1 V) at drain and sweeping voltage (from -1 to +1 V) between gate and source (ground) electrodes are applied. In case of current (*I*) – voltage (*V*) curves, constant gate voltage and sweeping voltage (0-1 V) between drain and source electrodes were applied. **Figure 3-8a** shows the transfer and *I-V* characteristics of 300 °C annealed sample. It shows that the operating voltages are low (±1 V) due to high capacitance of electrolyte. The transfer curve shows that the device is in the off state at negative gate voltages and starts to switch on at a threshold voltage and rises to the maximum attainable currents saturating at around 1 V. When the gate voltage is negative (or less than the threshold voltage), positive ions (K^+) of the electrolyte migrate towards the gate-electrolyte interface, whereas negative ions (F^-) migrate towards the semiconductor-electrolyte interface. These negative ions repel the electrons of the semiconductor and cause a depletion layer. As a result the device is in the off state. However, when the gate voltage is more than the threshold voltage (i.e.,

positive), negative ions migrate towards the gate and form an electrical double layer. At the same time, positive ions of the electrolyte migrate towards the semiconductor-electrolyte interface and form an electrical double layer with the electrons of the semiconductor. This creates an accumulation layer and the electrons start to flow from source to drain when a voltage is applied at the drain. The transfer curve shows that the device is in accumulation mode (positive threshold voltage, V_T = 0.15 V) and high drain currents (I_D = 0.8 μA/μm) and the calculated field effect mobility (using equation 2.1) is 23 cm^2/Vs. However, a negative differential resistance (NDR) effect (decrease in current with increase in voltage) is observed in the *I-V* curves, which is due to the presence of the insulating secondary phase InOCl. Transfer and *I-V* curves of 400 °C annealed sample are shown in **Figure 3-8b**. It is also in accumulation mode (V_T = 0.37 V) with a high drain current of 0.4 mA ($W/L \approx$ 3) and a mobility of 126 cm^2/Vs. Another merit of this device is that subthreshold slope is 68 mV/decade which is very close to the theoretical limit (60 mV/decade). This outstanding result is due to the large crystallite size (less scattering effects) and also very good interface between indium oxide and electrolyte, which has strong influence on the charge accumulation. For the 500 °C annealed sample, transfer and *I-V* curves **Figure 3-8c** shows accumulation mode (V_T = 0.16 V) and good saturation currents but the mobility (63 cm^2/Vs) is lower than that of the sample heat treated at 400 °C, which is due to smaller crystallite size and little rough film. **Table 3-2** summarizes the device parameters of all three samples. The transfer curves of all three samples show some hysteresis, which is due to the in-plane geometry of the transistor. In this geometry, the gate electrode is more than 50 μm far from the channel, which means that the charge carriers may not follow the same path while charging and discharging. This issue could be solved by incorporating a top gate electrode. Silver nanoparticulate as well as poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) inks have been used as top gate electrodes. However, the solubility of these inks with the solvents of the electrolyte has led to electrical contact with the channel. This increases the leakage currents significantly. Hence, a systematic study is necessary to solve this issue, which is outside the scope of this thesis. Another noticeable issue in the transfer curves of the devices is that the leakage currents are a little higher (i.e., few nanoamperes (nA)) than Si-based transistors. It might be due to the parasitic or unwanted currents from the passive electrodes (i.e., ITO). Minimizing the overlap area of the source-drain electrodes with the electrolyte can reduce the parasitic currents. This idea has been explored and the results are presented in the following chapters.

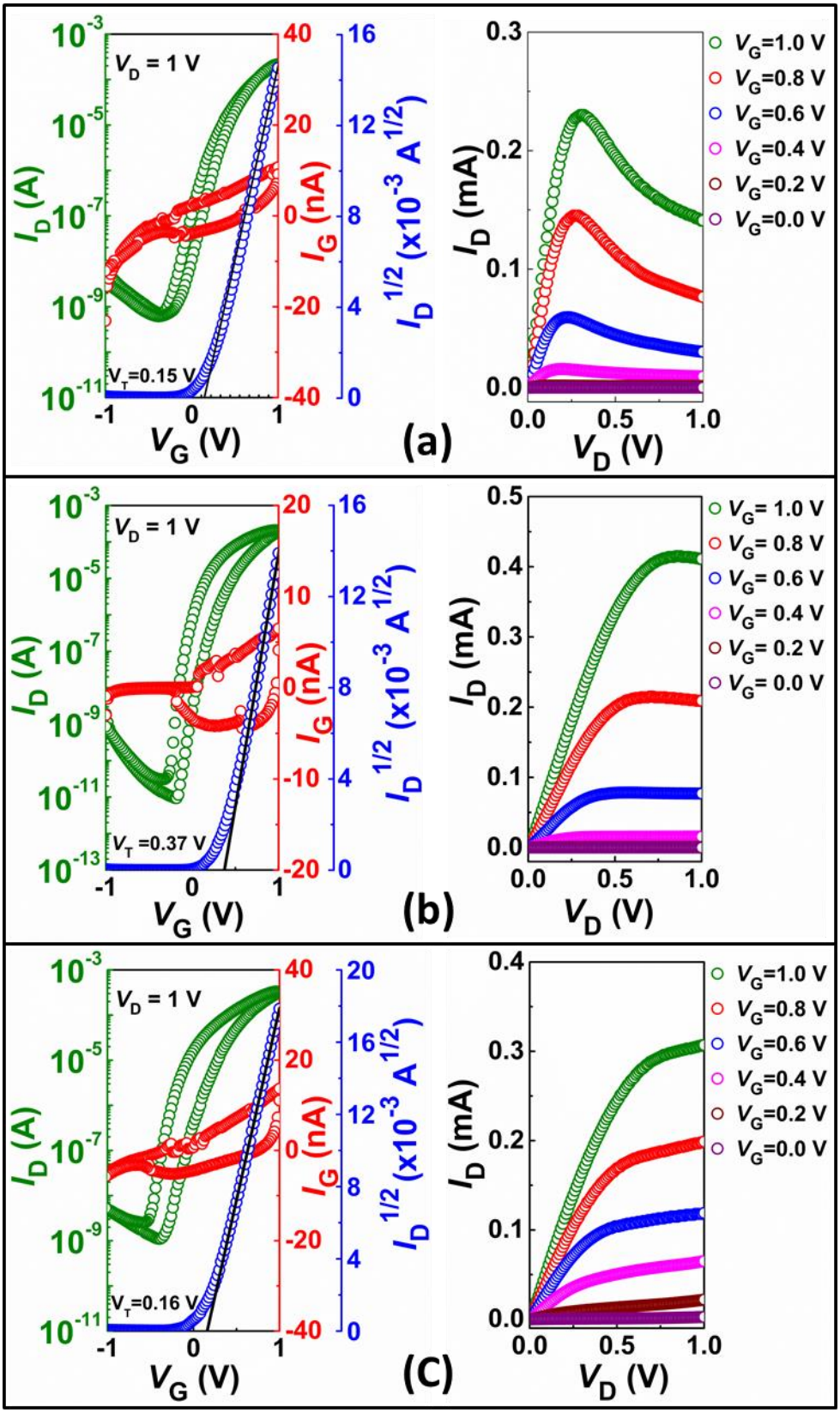

Figure 3-8 Transfer and *I-V* curves of the indium oxide precursors after annealing at (a) 300 (b) 400 and (c) 500 °C. The transfer curves (left side) show the drain current (I_D, green circles), the gate current (I_G, red circles), the square root of drain current ($I_D^{1/2}$, blue circles) on y-axis and the gate voltage (V_G) on the x-axis. The *I-V* curves (right side) show the drain current curves with a gate voltage variation from 0 to 1 V with a step size of 0.2 V (bottom to top) and the drain voltage (V_D) on x-axis.

T (°C)	ON/OFF ratio	I_D/W (μA/μm)	V_T (V)	SS (mV/decade)	G_m (μS/μm)	μ_{FET} (cm^2/(Vs))
300	3×10^5	0.8	0.15	126	2.7	23
400	2×10^7	2.4	0.37	68	3.3	126
500	3×10^5	2.4	0.16	126	5.5	63

Table 3-2 The transistor characteristics of the precursor based indium oxide FETs. The table shows the annealing temperatures of indium oxide precursors, the ON/OFF ratios, the ratios of drain current and channel width, the threshold voltages, the subthreshold slopes, the transconductances, and the field-effect mobility values.

The field effect mobility values are calculated from equation 2.1. All parameters are known except the capacitance (C), which in this case is the double layer capacitance ($C = C_{dl}$) of the channel. To find out the value of C_{dl}, a good quality film over a large area is required, which is difficult in printed precursor films due to accumulated ink while printing large areas and there by high thickness which in turn created cracks in the films. However, sputtered indium oxide films can also be used to determine the value of C_{dl}. Radio frequency magnetron sputtering is used to sputter indium oxide films (120 nm thick) from a commercially available indium oxide target. A parallel plate capacitor (PPC) to measure the C_{dl} is prepared using ITO and In_2O_3 as the counter electrode and working electrodes, respectively. The PPC is prepared in such a way that the area of counter electrode is much larger (≥ 5 times) than the working electrode, which makes sure that the charging current comes only from the working electrode. Cyclic voltammetry (CV) measurements are performed for this PPC at different scan rates (0.01-0.5 V/s) with a potential window of ± 0.1 V (**Figure 3-9a-d**). CV measurement graphs indicate that the current density is nearly constant within the potential window, which indicates that there is no chemical reaction. However, current density increases with scan rate, which is due to the increase in charge density, i.e. higher the scan rate, higher the time for charge accumulation. Using the same graphs, the capacitance (current/scan rate) value can be estimated as 3.75 μF/cm^2. However, to have a better estimation of the capacitance at high voltages, impedance measurements have also been performed at different frequencies (0.1-1000 Hz) with a potential window of 0-1 V (**Figure 3-10**). It shows that the capacitance decreases heavily at higher frequencies, which can be due to large distances (≈ 2 mm) between the two electrodes of the cell, not the case for real devices. The capacitance value is calculated at the lowest frequency of 0.1 Hz and at 1 V gate voltage. The obtained capacitance value is 4.33 μF/cm^2, which is determined using the following equation:

$$C_{eff} = \frac{-Z''}{\omega |Z|^2} \qquad (3.2)$$

where C_{eff} is the effective capacitance, Z'' is the imaginary part of the impedance, |Z| is the impedance modulus, ω is the angular frequency [100]. The lowest frequency and high gate voltages have been chosen to obtain a rather large capacitance value, which on the other hand will provide a conservative estimation of the calculated field-effect mobility. On the other hand, as shown in **Figure 3-10** the capacitance value does not change significantly with gate potential. This is due to the fact that for the sputtered films the initial doping (carrier) concentration is too large to observe real gate dependence like a typical semiconductor. With this capacitance

value, the calculated field-effect mobility value is as high as 126 cm^2/Vs. The large crystallite size and smooth interface contributed to obtain this high performance.

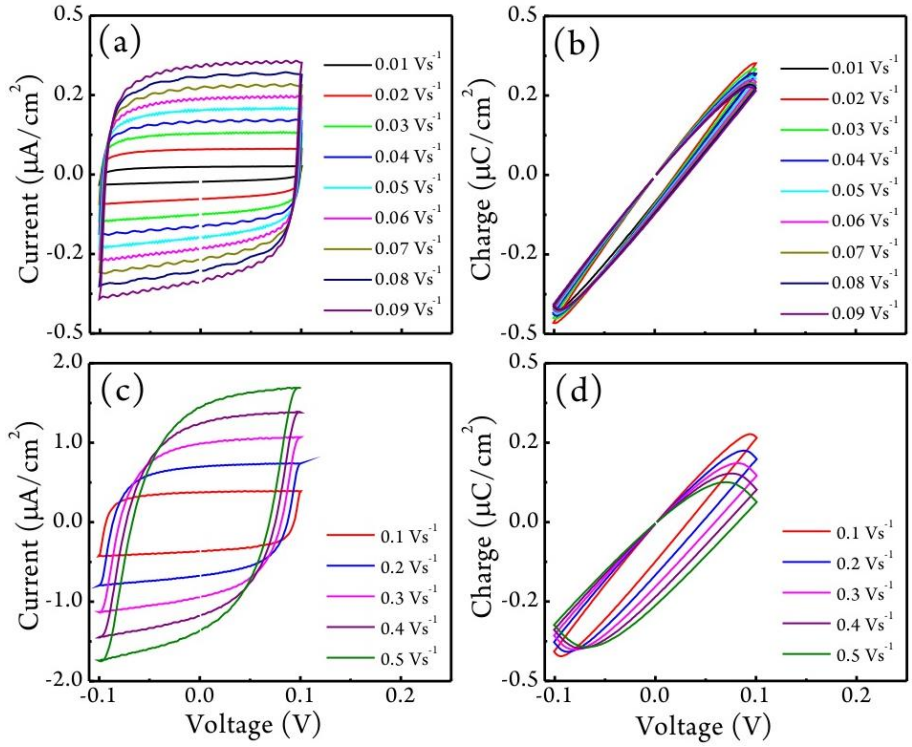

Figure 3-9 Cyclic voltammetry measurements of indium oxide using electrolyte and ITO as the counter electrode which shows current density (a and c) and accumulated charge (b and d) at different scan rates (0.01-0.5 V/s)

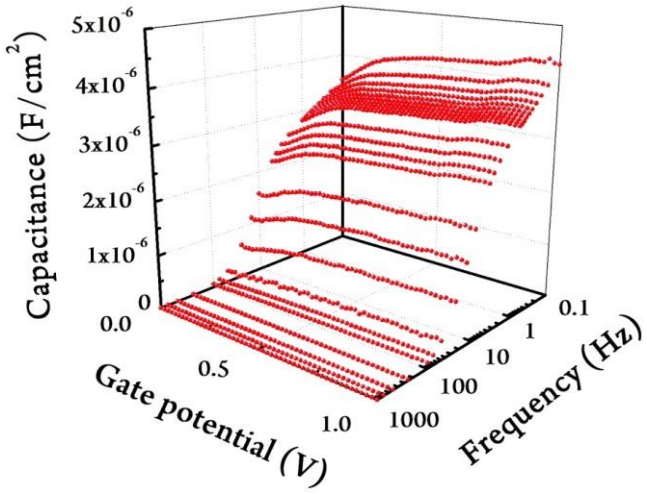

Figure 3-10 Impedance measurements of indium oxide using electrolyte and ITO as the counter electrode, at different frequencies (0.1-1000 Hz) with a gate potential of 1 V. It shows the variation of capacitance with respect to frequency as well as gate potential.

3.1.3. Effect of annealing conditions on the performance of transistors

To demonstrate the effect of annealing conditions on the performance of the FETs, two substrates with indium oxide channels, which were printed using the same precursor and identical printing conditions, are annealed at 500 °C for 1 h with very slow (1 °C/min) and fast heating rates (directly inserted at that temperature and taken out after 1 h). After annealing, the electrolyte is printed on the devices and electrical characterization is carried out. Transfer and *I-V* curves of slow heating devices are already shown in **Figure 3-8c** and for fast heated sample it is shown in **Figure 3-11**. It clearly shows that drain current is lower and so is the mobility (51 cm^2/Vs). This result is attributed to the lower crystallite size (86 nm) and also poor film quality, which is due to the sudden change in the temperature of the printed film while heating and cooling. For the comparison, XRD patterns of both the samples are shown in **Figure 3-12**. These XRD patterns indicate that indium oxide forms at both heating rates. However, a slow heating rate is the best way to obtain large crystallite size as well as good film quality and electrical performance. On the other hand, the overall heating time at slow heating rates is more than 16 times longer than for fast heating rates. Therefore, a compromise between heating rate and performance may be necessary if the concept is considered for commercial applications.

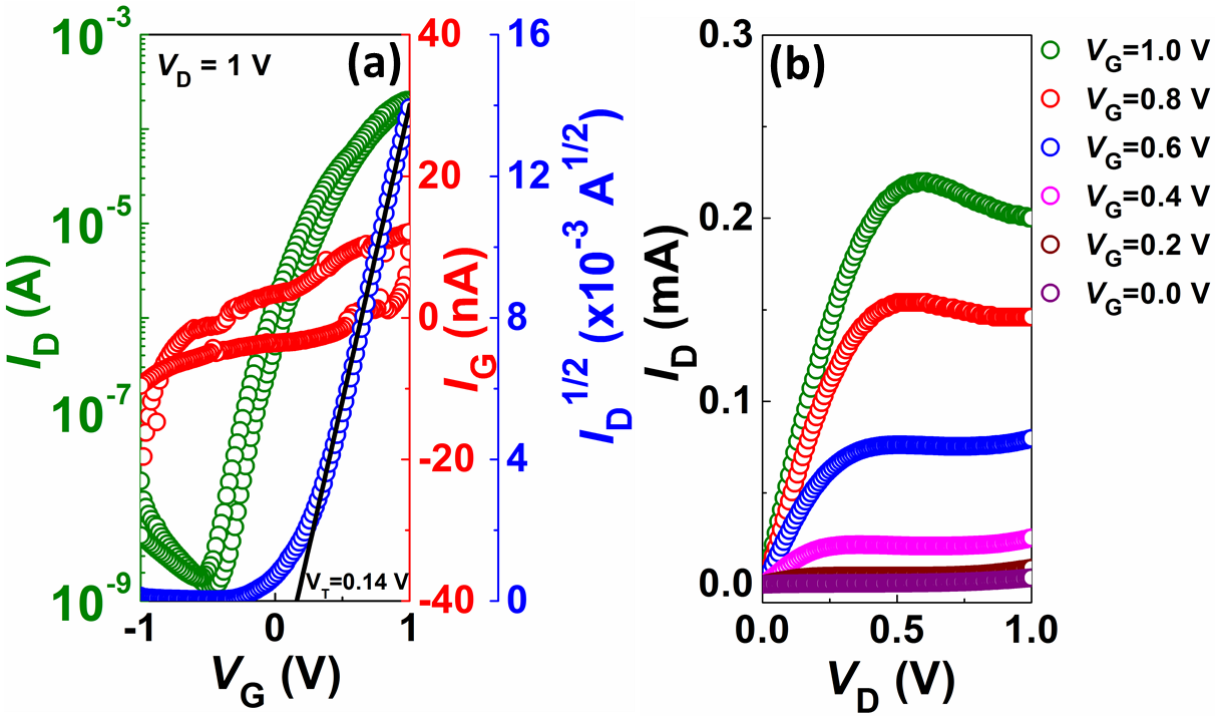

Figure 3-11 (a) Transfer and (b) *I-V* curves of the sample after fast heating to 500 °C. The drain current (I_D, green circles), the gate current (I_G, red circles), the square root of drain current ($I_D^{1/2}$, blue circles) and the gate voltages (V_G) are shown in the transfer curve. The *I-V* curves show the drain current curves with a gate voltage variation from 0 to 1 V with a step size of 0.2 V (bottom to top) and the drain voltages (V_D).

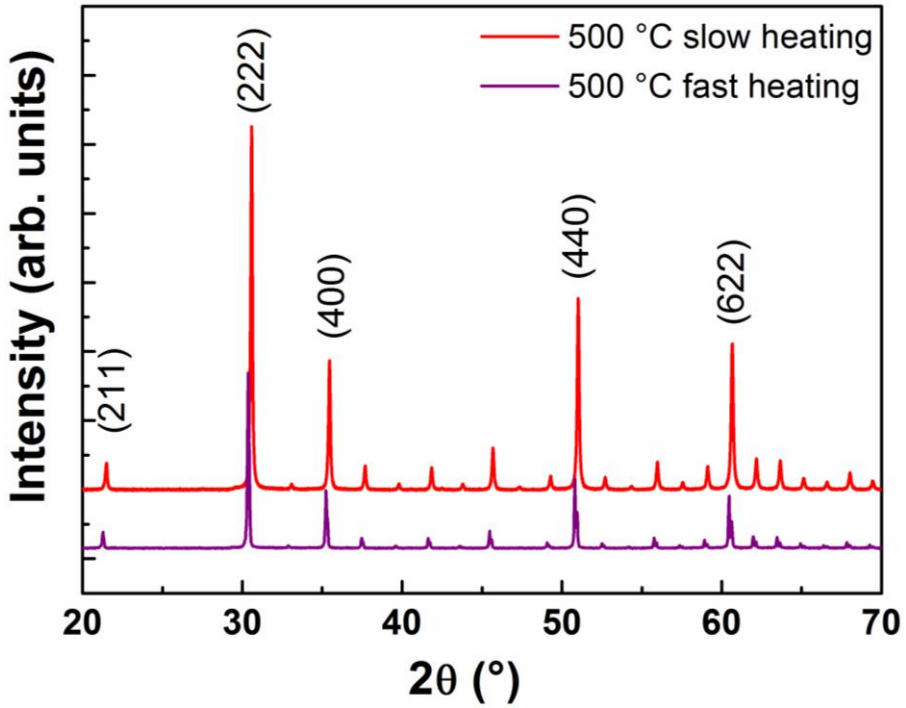

Figure 3-12 XRD patterns of samples after slow and fast heating (at 500 °C) of the indium oxide precursor.

In summary, inkjet printed and electrolyte gated indium oxide FETs using precursors, which are annealed at different temperatures (300- 500 °C) and also with different heating rates (1 °C/min and directly inserted at that temperature) have been prepared. Structural characterization showed clearly that difference in crystallite sizes and film morphologies due to different heating conditions. Consequently, the performance of FETs is also affected by the annealing conditions. Nevertheless, the best performance, i.e. high field effect mobility and close to theoretical limit of subthreshold slope are obtained for the precursor annealed at 400 °C due to large crystallite size, good film quality, and smooth interface with electrolyte.

3.2. Complementary metal oxide semiconductors electronics using n- and p-type oxide precursors

Hitherto, single oxide transistors have been prepared. However, it is necessary to investigate multiple FETs and their combination for the realization of complex logic circuits. One such attempt has been made here using n- and p-type oxides. In this section, a CMOS inverter and a common source amplifier are demonstrated using precursors of n-type In_2O_3 and p-type CuO.

3.2.1. Preparation of complementary metal oxide semiconductors devices

In this study, nitrate salts are chosen due to their lower decomposition temperatures compared to chlorides. 0.05 M indium nitrate hydrate ($In_2O_3 \cdot xH_2O$) and 0.1 M copper nitrate hemi pentahydrate ($Cu(NO_3)_2 \cdot 2.5H_2O$) were dissolved in a mixture of water and glycerol (volume ratio of 4:1) separately. These sols were then filtered through 0.2 μm PVDF membrane filters. Next, in-plane passive structures of FET were prepared on silicon wafer (Si/SiO_2) using lithography and sputtered Cr (10 nm) / Pt (30 nm) as the electrodes. Channel lengths were fixed to 100 μm and 10 μm for NMOS and PMOS, respectively. On these structures, both the precursors were printed and dried at 150 °C for 2-3 min and annealed (heating rate of 5 °C/min) at 400 °C for 2 h. Optical microscopy is used to determine the width of the channels. The approximate width to length ratio (*W*/*L*) of NMOS and PMOS has been chosen as 1 and 7, respectively. In parallel, CSPE is prepared in the following procedure: lithium perchlorate ($LiCLO_4$) is dissolved in propylene carbonate (PC) at RT and PVA (molecular weight of 13000-23000 g/mol) is dissolved in dimethyl sulfoxide (DMSO) at 80 °C and then these two solutions are mixed together thoroughly. Next, the CSPE solution is filtered through 0.45 and 0.2 μm Polytetrafluoroethylene (PTFE) membrane filters. The concentration of the ingredients is optimized to obtain good performance of the electrolyte and the ratio of PVA:PC:$LiClO_4$ is kept at 30:63:7, to ensure that the viscosity of the electrolyte lies within the suitable range for inkjet printing. The weight of DMSO is taken 6 times more than the total weight of all the other components together. The prepared electrolyte is printed on annealed channels at RT and allowed to dry at ambient conditions.

For the structural characterization, a similar batch of Si wafers was used. Precursor droplets were solution casted on these wafers, which were then dried and annealed at identical conditions. These samples have been characterized by grazing incidence XRD (Mo Kα source) with a fixed incident angle of 0.4°. For SEM (Zeiss Leo 1530) and AFM (Bruker dimension icon) analyses, printed channels without electrolyte were used. Similarly, samples for cross-section transmission electron microscopy (TEM, TITAN 80-300 kV) analysis were prepared by focused ion beam (FIB, FEI Strata 400S dual beam). The electrolyte was solution cast onto annealed indium oxide samples. After drying the electrolyte at ambient conditions, a 50 nm gold film was deposited by sputtering technique. In FIB, 10 nm of Pt is deposited on a selected area and then 2 μm Pt is

deposited using gas injection ion beam system (GIS). Subsequently, cross-section samples were prepared in the form of a thin lamella by milling and fine polishing. Because the electrolyte can be damaged by the beam, great care was taken while preparing the sample. The prepared lamella was lifted using an Omniprobe system and further thinned for transmission electron microscopy TEM investigation. FEI Titan 80-300 TEM was used to analyze the interface.

3.2.2. Structural Characterization

The phase formation of the annealed precursors is analyzed by grazing incidence XRD. The results are shown in **Figure 3-13**. The XRD patterns show that crystalline indium oxide is not formed below 300 °C. Indium oxide is formed at 300 °C. The crystallinity increases further at 400 °C. The formation of indium oxide can be explained by a simple sol-gel reaction, i.e., dissolved indium nitrate forms indium hydroxide ($In(OH)_3$) after drying, which decomposes to indium oxide at high temperatures (≥ 300 °C). Whereas for cuprous oxide precursor, pure copper is observed at 150 °C, which is due to the reducing agent glycerol. It was earlier reported that in polyol process glycols and glycerol can act as reducing agent to obtain pure metals from their salts [106]. At 300 °C, copper started to oxidize to Cu_2O but still significant amount of copper was present. At 400 °C, copper completely oxidized to its higher oxidation state CuO with some secondary Cu_2O phase. On the other hand, Cu_2O is also a p-type semiconductor, so it may not be detrimental. Rietveld refinements for the precursors, after annealing at 300 °C and 400 °C have been performed using "Fullprof" software with Pseudo-Voigt method (**Figure 3-14**). The calculated amount of Cu_2O of the sample, which is annealed at 400 °C, is approximately 10% (**Table 3-3**). The amount of this secondary phase can be further reduced by heating at even higher temperatures, because Cu_2O oxidizes to CuO at higher temperatures. However, the maximum temperature that the known plastic substrate (for example kapton) can sustain is 400 °C. Hence, to realize logics on flexible substrates, the processing temperature has to be ≤ 400 °C. Next, to further corroborate the particle size as well as particle morphology cross-section SEM images have been taken (**Figure 3-15**). These images indicate that the films are smooth and the particle sizes are comparable to the calculated values. In fact, indium oxide can be used at lower temperatures (~230 °C) using indium acetate precursor (**Figure 3-16**), however, cuprous oxide is not formed until 400 °C and to make the process simple, just one step heating has been used.

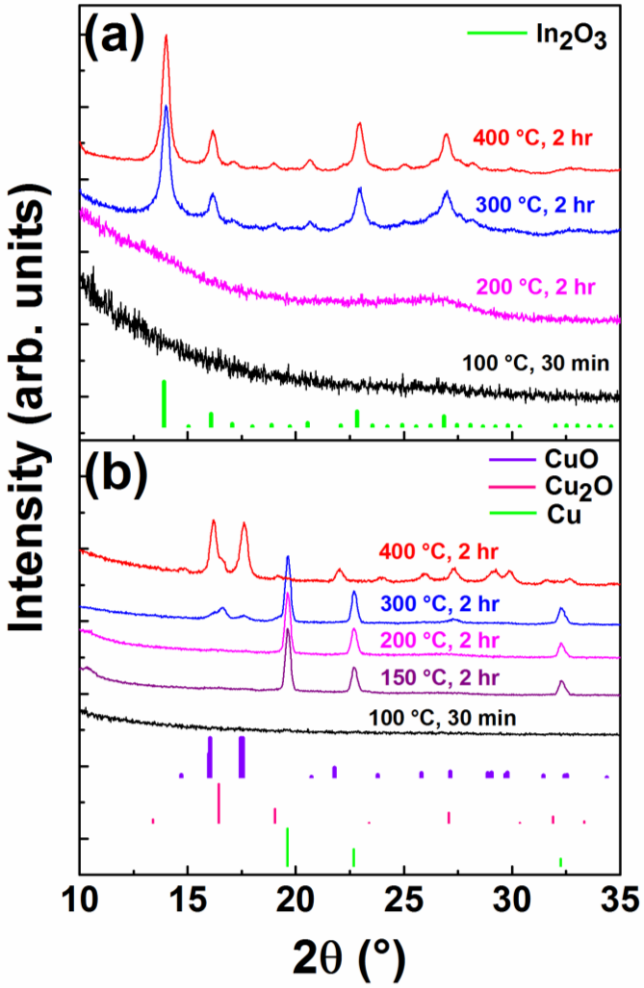

Figure 3-13 XRD patterns of indium oxide and cuprous oxide precursors after annealing at different temperatures. The vertical lines correspond to the standard reference patterns of In_2O_3, Cu, Cu_2O and CuO.

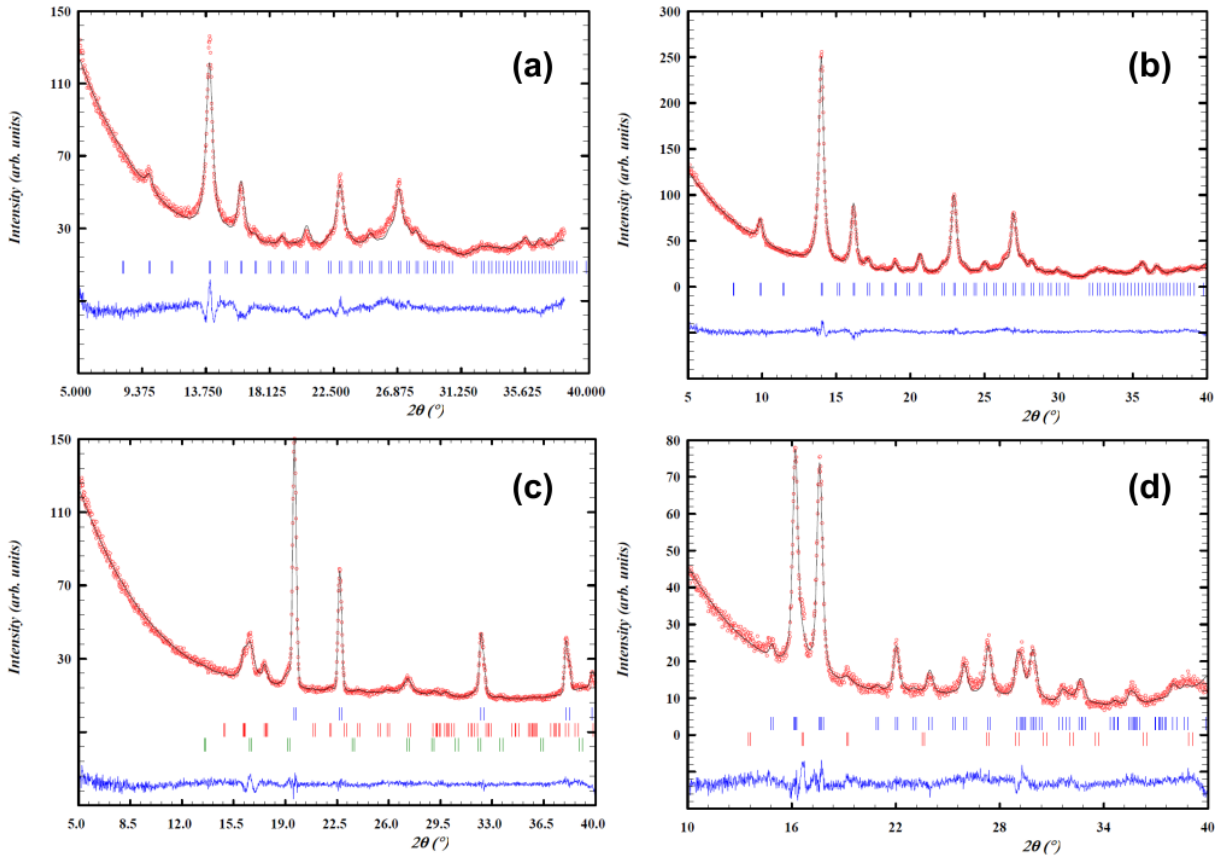

Figure 3-14 Rietveld refinement of the XRD data of printed indium oxide and cooper oxide thin films where the In_2O_3 precursors have been annealed at (a) 300 °C and (b) 400 °C, respectively; similarly, (c) and (d) correspond to CuO precursors that have been heated to 300 °C and 400 °C, respectively.

Temperature (°C)	Crystallite size (nm)		Fraction of phases (%)		
	In_2O_3	CuO	Cu	Cu_2O	CuO
300	12.5	-	50	38	12
400	14.7	14.7	-	10	90

Table 3-3 Crystallite sizes and fraction of phases of indium oxide and cuprous oxide precursors which are annealed at 300 and 400 °C.

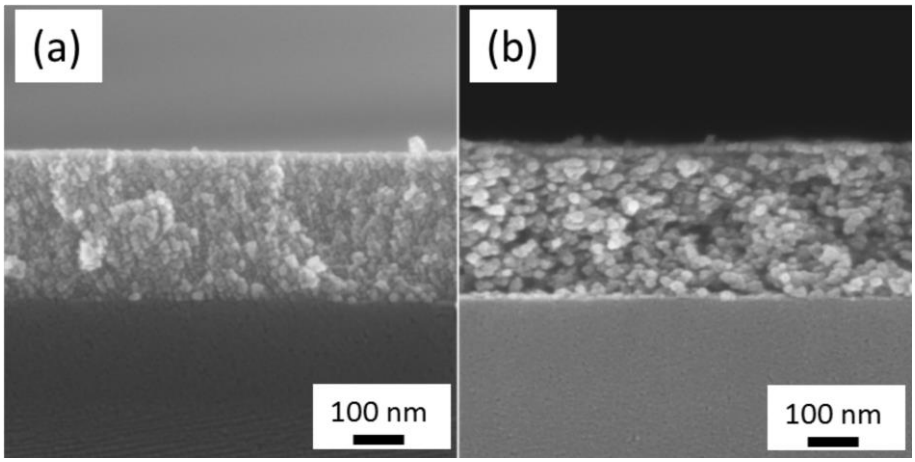

Figure 3-15 Cross-section SEM images of (a) In_2O_3 and (b) CuO films. It shows (bottom to top) substrate, oxide film and no material region.

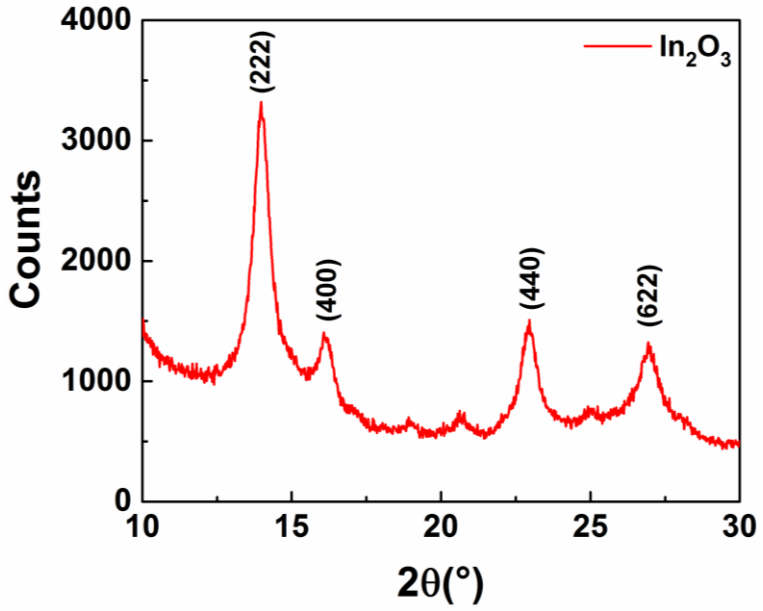

Figure 3-16 XRD pattern of indium oxide precursor which is annealed at 230 °C. Miller indices (atomic planes) of standard indium oxide are also shown for high intense peaks.

The morphology of the annealed (400 °C) films was characterized by SEM and AFM as shown in **Figure 3-17**. It shows that indium oxide films are highly homogeneous, extremely smooth (roughness is just about 0.5 nm). This may be due to direct nucleation of indium oxide from nitrate salts without any intermediate product and also the addition of glycerol (which has high boiling point and viscosity) may have helped. On the other hand, cuprous oxide films have large particles and they seem to be little rough (roughness is 9 nm), which might be due to the initial nucleation of copper followed by its oxidation. Both surface roughness and section analysis of indium oxide as well as copper oxides films are shown in **Figure 3-18** and **Figure 3-19**, respectively. Section analysis also clearly shows that the indium oxide films are smoother than the copper oxide films. Furthermore, to investigate the interface of semiconductor and electrolyte, TEM analysis on a cross-section sample of indium

oxide and CSPE was performed and **Figure 3-20** shows crystalline indium oxide nanoparticles and the associated lattice fringes that are obtained from the fast Fourier transformation (FFT). This cross-section image clearly shows that the electrolyte is completely following the indium oxide surface roughness down to nanometer level, and such a smooth interface can obviously lead to high gating efficiency.

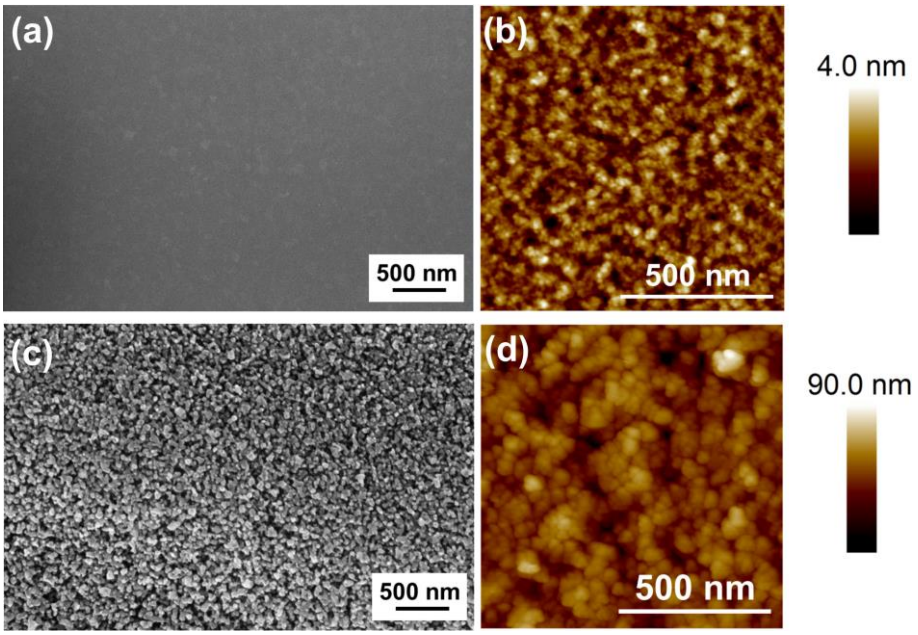

Figure 3-17 SEM and AFM images of indium oxide (a & b) and copper oxide (c & d) precursor films after annealing at 400 °C for 2 h in air, respectively.

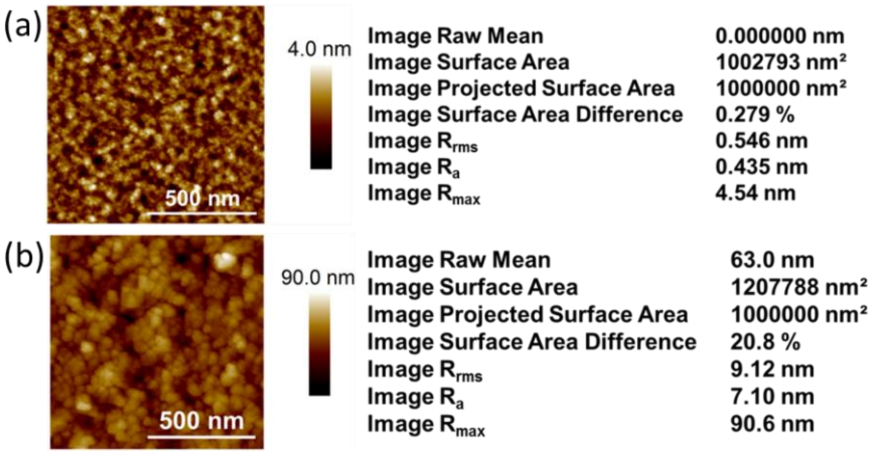

Figure 3-18 Surface roughness analysis of AFM micrographs of (a) indium oxide and (b) copper oxide precursor derived thin films, which are annealed at 400 °C for 2 h in air. In the roughness analysis, image raw mean is the mean value of image data without application of plane fitting, image surface area is the three-dimensional (3D) area of the image, image projected surface area is the area of the image rectangle, image surface area difference is the difference between the image's 3D surface area and the projected surface area, R_{rms} is the root mean square average of height deviations taken from the mean data plane, R_a is average roughness, R_{max} is the maximum vertical distance between the highest and lowest data points in the image [105].

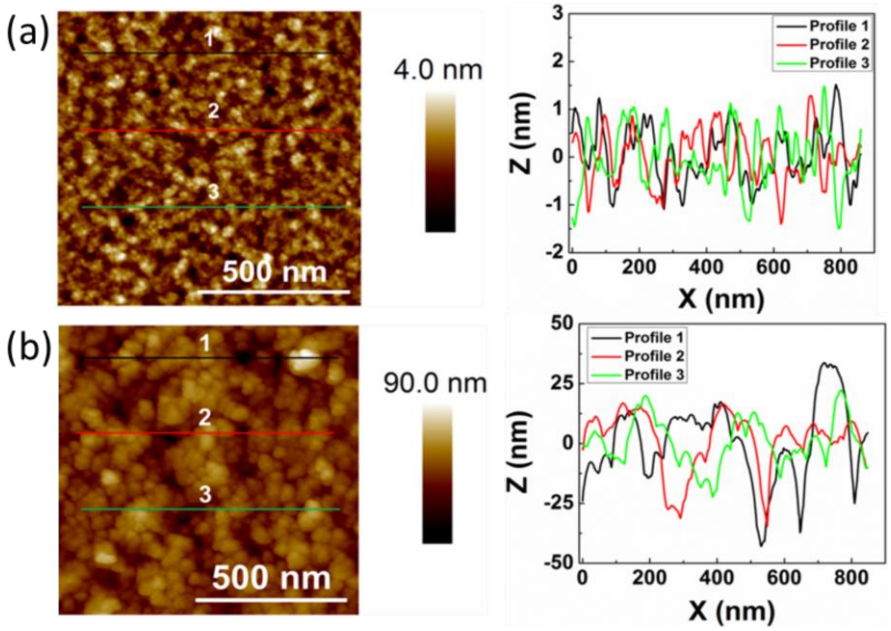

Figure 3-19 Section analysis of AFM micrographs of (a) indium oxide and (b) copper oxide precursor derived thin films, which are annealed at 400 °C for 2 h in air.

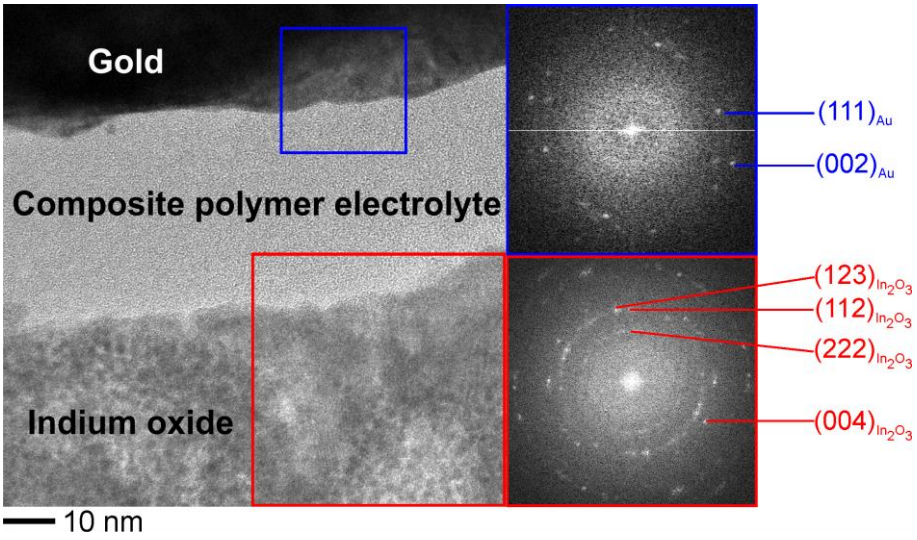

Figure 3-20 Cross-section TEM image of the interface between indium oxide and composite solid polymer electrolyte. The fast Fourier transforms of indium oxide and gold are shown in red and blue rectangles.

3.2.3. Electrical characterization of complementary metal oxide semiconductor inverter and common source amplifiers

The prepared NMOS and PMOS FETs are characterized at ambient conditions (i.e. room temperature and ambient atmosphere). The transfer and *I-V* curves are shown in **Figure 3-21**. The NMOS transfer curve shows that it is in accumulation mode (V_T = 0.32 V) with high drain current (0.29 mA) and high ON/OFF ratio (10^6). The calculated field effect mobility is 48 cm^2/Vs and subthreshold slope is also sharp (100 mV/decade). The

field-effect mobility of this device is less than the devices that are presented in the previous section. It might be due to many factors such as difference in the channel lengths (100 and 50 μm for the present and previous NMOS), electrode materials and also difference in crystallite size of the indium oxide films, i.e., 101 nm and 14.7 nm for earlier and the present films, respectively. However, to obtain a high performance CMOS inverter, it is necessary to match the performance of NMOS with PMOS. Therefore, a low mobility NMOS is suitable to match the performance of the PMOS. On the other hand, the PMOS shows accumulation mode (V_T = -0.23 V) with ON/OFF ratio and subthreshold slope of 10^3 and 600 mV/decade, respectively. *I-V* curves of PMOS show the presence of Schottky contacts (although a high work function (> 5 eV) electrode (Pt) is used), which might be due to secondary phase of copper oxide films. Furthermore, the *I-V* curves are not saturated even at higher voltages, and the reasons for this behavior are not clear. However, it might be due to the in-plane design of the FET and also low mobility of the charge carriers (holes). It has been already mentioned that p-type oxides have low mobility due to a localized valence bond which is formed from oxygen 2p orbitals. Nevertheless, the achieved field effect mobility of PMOS is 0.22 cm^2/Vs, which is comparable to epitaxially grown PMOS FETs [107]. On the other hand, indium oxide can be prepared at lower temperatures (230 °C for 1 h in air) and the corresponding transistor characteristics are shown in **Figure 3-22**. Transfer curves show that the devices are in enhancement mode (V_T= 0.5 V) with ON/OFF ratio of 10^7 and sharp subthreshold slope (80 mV/decade). Although, the achieved field-effect mobility (8.3 cm^2/Vs) is somewhat lower than 400 °C annealed devices, this may very well be useful for some low temperature applications. On the other hand, copper oxide is not formed at lower temperatures and it limited the preparation of CMOS inverter at lower temperatures.

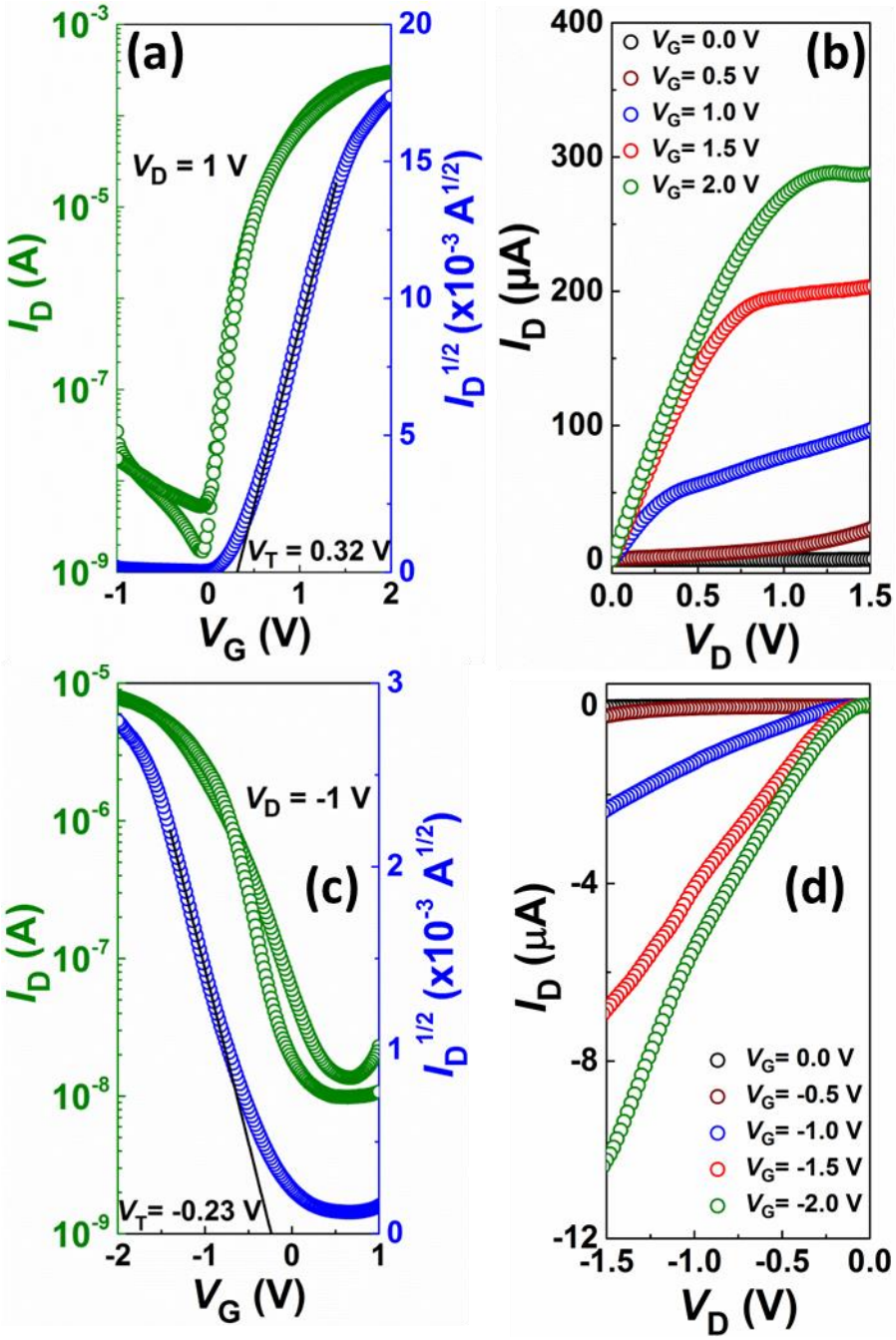

Figure 3-21 Transfer and *I-V* curves of NMOS (a & b) and PMOS (c & d) FETs, respectively. The transfer curves show the drain current (I_D, green circles), the square root of drain current ($I_D^{1/2}$, blue circles) with a linear fit (black line) and the gate voltages (V_G). In the *I-V* curves, the drain voltage (V_D), and the drain current curves (I_D, black to green circles) with the variation of the gate voltage (V_G from 0.0 to 1.0 V with a step size of 0.5 V) are shown.

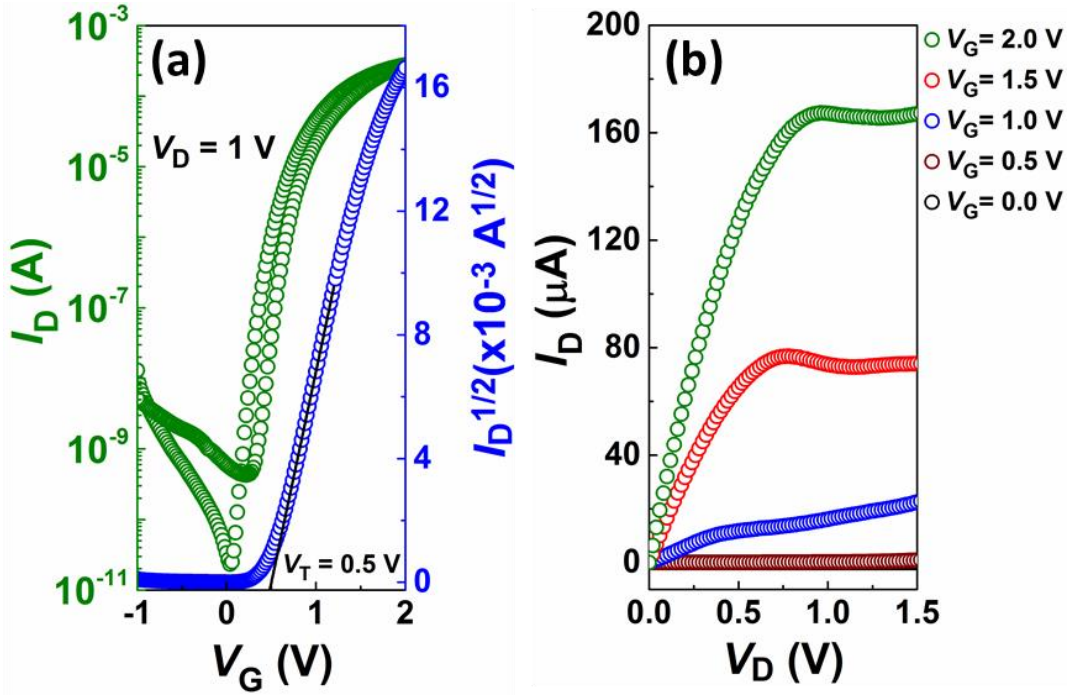

Figure 3-22 (a) Transfer and (b) *I-V* curves of indium oxide precursor (annealed at 230 °C for 1 h in air) based FET.

Field-effect mobility values are calculated using equation 2.1, in which most of the parameters are known except capacitance. To measure the capacitance, separate NMOS devices using ITO as electrodes were prepared with similar *W*/*L* ratio under same preparation conditions. Electrolyte was printed very carefully so that overlap with ITO electrodes is less, thereby parasitic currents are low. The displacement/charging currents are measured with different gate voltage scan rates (**Figure 3-23a**). The displacement current resulting mainly from the semiconducting material can give the exact value of C_{dl}. Next, the current density can be obtained by dividing the observed displacement current by the printed area. A simple parallel plate capacitor model gives charge (Q) proportional to the voltage drop (V) across the capacitor, *i.e.:*

$$Q = CV \qquad (3.3)$$

Differentiating equation (3.3) with respect to t gives:

$$\frac{dQ}{dt} = C\frac{dV}{dt} \qquad (3.4)$$

where $\frac{dQ}{dt}$ is the said current density, *i.e.* the displacement current resulting from the unit area of the semiconductor and $\frac{dV}{dt}$ is the voltage scan rate, υ. Therefore:

$$i = C\upsilon \qquad (3.5)$$

Following equation (3.5), the slope of **Figure 3-23b** gives the specific capacitance of the channel. Charging/displacement current vs gate voltage graphs curves with different scan rates (10-40 mV/s) are used to estimate the double layer capacitance of indium oxide films. The estimated value of C_{dl} is 4.63μF/cm^2. However, an estimation of C_{dl} of copper oxide using the same method is not possible. As already mentioned above, an accurate estimation of C_{dl} from the displacement current is only possible when the parasitic currents

from the passive structures are negligible. Since, CuO is a p-type semiconductor, a high work function metal such as Pt should be used as the electrode. However, Pt gives considerable parasitic currents. Therefore, a different approach has been followed, i.e., large-area parallel plate capacitors were built with sputtered CuO thin films and with sputtered platinum as the counter electrode. The composite polymer electrolyte was solution cast between the electrodes and dried at ambient conditions. Cyclic voltammetry measurements were carried out to observe the displacement currents (**Figure 3-24**). Copper oxide has low hole mobility: as a result, the electrolytic charging is incomplete even for a scan speed of 0.1 V/s, as can be seen in **Figure 3-24a**. Therefore, in this case, the CV measurements were conducted at relatively low scan speeds 0.02-0.1 V/s. The calculated specific capacitance of copper oxide at a scan speed of 0.1 V/s (identical to the speed of FET measurements) is found to be 3.2 µF/cm^2. Although, CuO has a low mobility, the specific capacitance is high due to high carrier concentration (close to 10^{19} cm^{-3}).

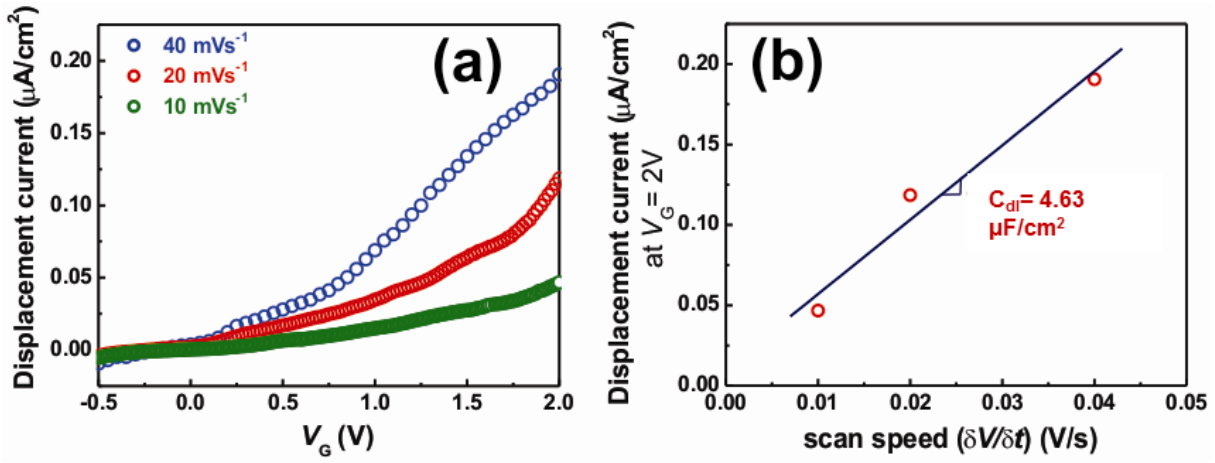

Figure 3-23 (a) Displacement current density at different gate voltage scan rates and (b) the displacement currents plotted vs scan rates; the slope of the fit provides the double layer capacitance.

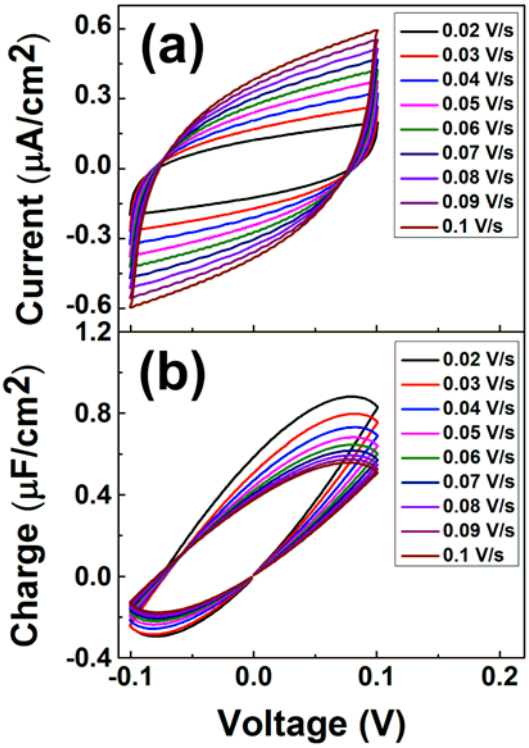

Figure 3-24 Cyclic voltammetry measurements at different scan rates are performed with sputtered copper oxide parallel plate capacitors; (a) displacement currents and (b) accumulated charge on the CuO electrodes, are presented.

Although, performances of NMOS and PMOS do not quite match each other, a clever geometry of a rather low performance PMOS can still lead to high signal gains. CMOS inverters and common source amplifiers are prepared by combing oxide semiconductors NMOS and PMOS: the corresponding optical images are shown in **Figure 3-25**. CMOS inverter curves (**Figure 3-26**) show that the devices can be operated at low voltages (≤ 2 V) owing to the high polarization of the electrolytic insulators. The CMOS inverter transfer curve (**Figure 3-26a**) shows that high output voltage is almost same as V_{DD}. It also shows a sharp transition of the transfer curves, which led to a signal gain of 21 at 1.5 V (**Figure 3-26b**) supply voltage and then close to zero output for a high input voltage. However, little high supply current (few hundreds of nanoamperes) is observed (**Figure 3-26c**) at the transition which is due to high capacitance of electrolyte. Although the achieved signal gain is higher than that reported for the CMOS inverter (using sputtered oxides) [108], it can be further improved by using high performance PMOS transistors. Alternative materials such as SnO, copper oxides doped with suitable materials, etc., have to be investigated for PMOS FETs. However, this is not the scope of the present thesis. Next, the dynamic power consumption (P) of the inverter can be calculated as

$$P = CV^2 f \qquad (3.6)$$

where C is capacitance, f is frequency, V is supply voltage [109]. The frequency of the present devices is not known and it might be lower than 1 kHz due to the in-plane geometry. However, the capacitance of electrolyte-gated devices is higher (i.e., microfarads) than dielectric oxide gated devices (usually nanofarads). This may

lead to high dynamic power consumption. On the other hand, further optimization of supply voltage as well as frequency (< 10 MHz, due to slow double layer formation) may lead to low power consumption. Another important parameter of CMOS inverters is noise margin. Calculated noise margins NM_H and NM_L are 0.57, 0.23 for 1 V and 1.15 and 0.09 for 1.5 V, respectively (**Figure 3-27**). It indicates that at 1 V, NMs are moderate but at 1.5 V, the deviation is little high when compared to an ideal case. However, the forbidden regions are 0.2 and 0.26 for 1 and 1.5 V, which is also an indication of good performance of prepared CMOS inverter. Another logic circuit, namely the common source amplifier, is also prepared by using same NMOS and PMOS. The curves (**Figure 3-28**) show a signal gain of 6 at 0.5 V with low supply current (30 picoamperes (pA)). However, optimization of these devices will ensure high signal gains and low power consumption.

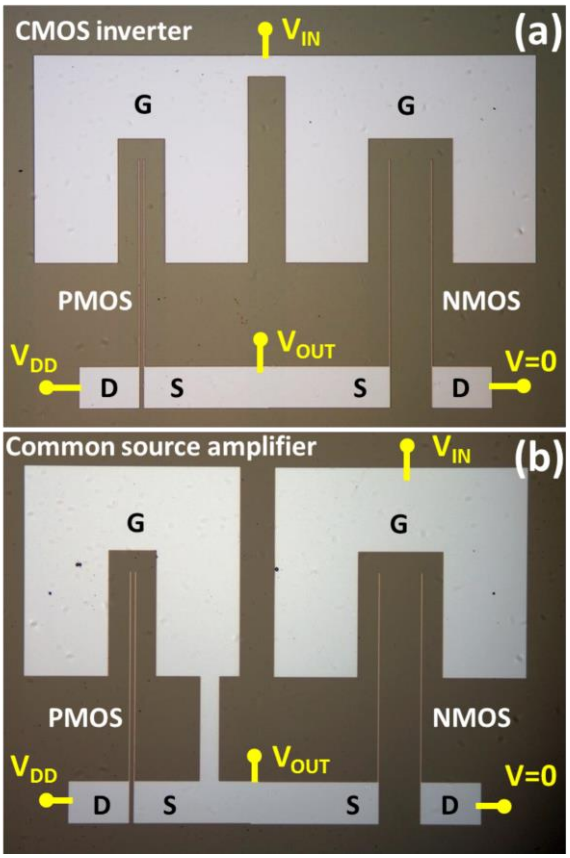

Figure 3-25 Optical images of (a) CMOS inverter and (b) common source amplifiers. Input (V_{IN}), output (V_{OUT}), drive or source (V_{DD}) and ground (V=0) voltages are shown for CMOS inverter and common source amplifiers.

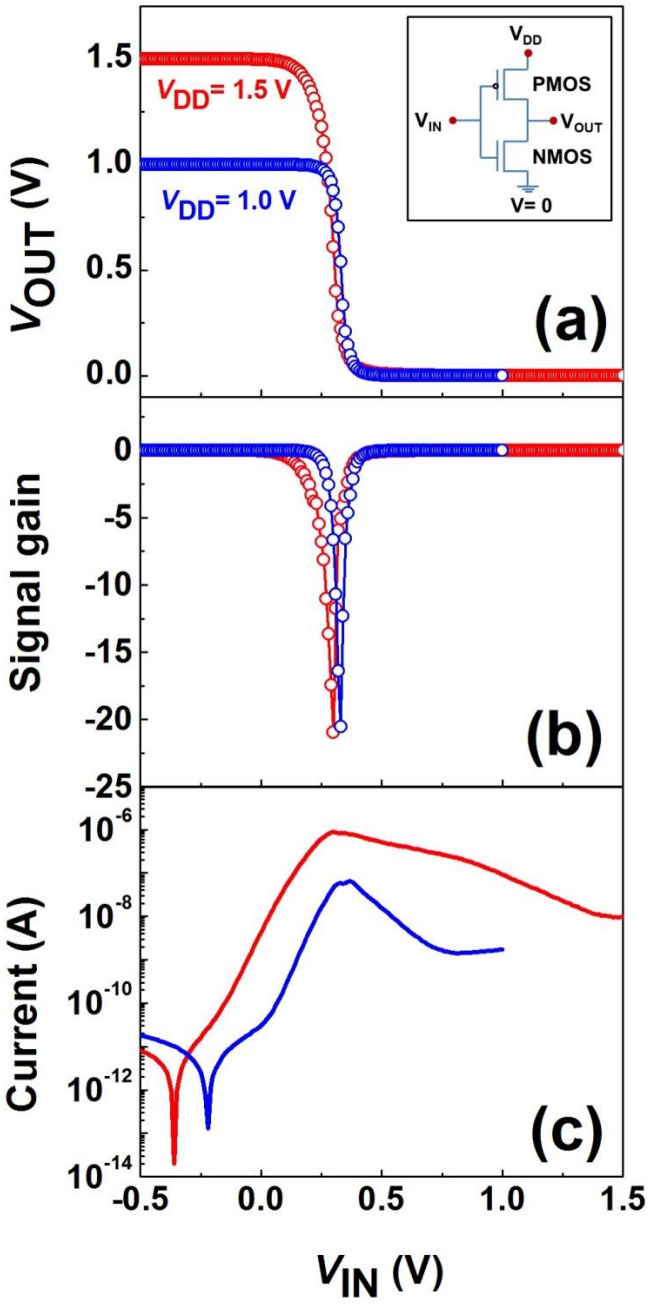

Figure 3-26 CMOS inverter (a) transfer (b) signal gain (c) supply current curves at 1 and 1.5 V of V_{DD}. The inset figure shows the circuit diagram of the CMOS inverter. Signal gain is negative due to the shift in the phase angle by 180 °C compared to the input of the measurement.

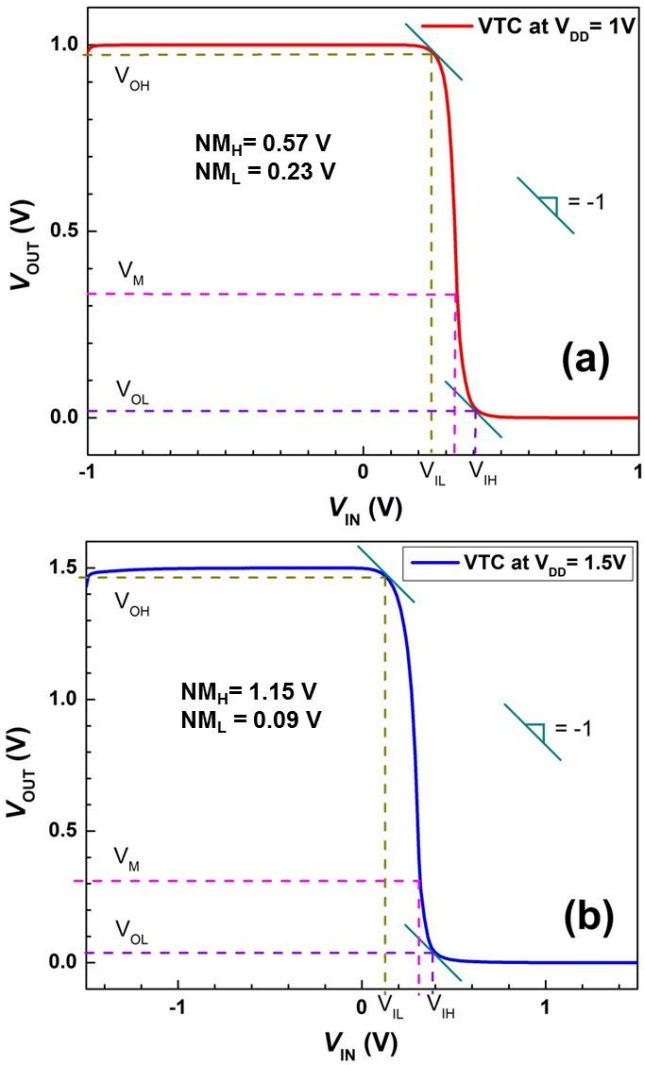

Figure 3-27 Noise margin graphs of CMOS inverter at (a) 1 V and (b) 1.5 V. It also shows the calculated high (NM_H) as well as low (NM_L) noise margins at 1 and 1.5 V of V_{DD}. The difference between minimum high output voltage (V_{OH}) and minimum high input voltage (V_{IH}) gives rise to NM_H, The value of NM_L is obtained by taking the difference of maximum low input voltage (V_{IL}) and maximum low output voltage (V_{OL}). Input and out voltages are equal at V_M.

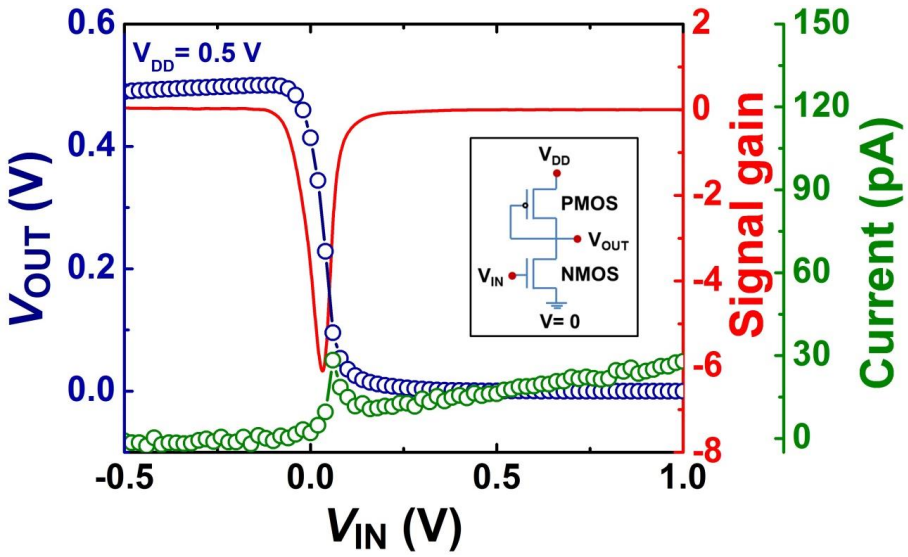

Figure 3-28 Voltage transfer (blue color circles with connecting lines), signal gain (red color line) and supply current (green color circles with connecting lines) curves of common source amplifier at a V_{DD} of 0.5 V. Circuit diagram is shown in the inset figure.

In summary, for the first time, CMOS inverter and common source amplifier logics have been prepared using oxide precursors. The printed precursors have been annealed at 400 °C for 2 h. Electrolyte gated In_2O_3 and CuO precursors are used to prepare NMOS and PMOS FETs, respectively. Structural characterization revealed the phase, composition and morphology of the films. Electrical characterization is also carried out and the calculated field effect mobility values are 48, 0.22 cm^2/Vs for NMOS and PMOS, respectively. The CMOS inverter showed a signal gain of 21 at 1.5 V with nominal power consumption. Calculated noise margins are also moderate at 1 V and deviated at 1.5 V when compared to the ideal case. Common source amplifier is also demonstrated, which showed a signal gain of 6 at 0.5 V with low power consumption.

4. Low/room Temperature Processed Oxide Electronics

It is clear that the high processing temperatures for oxide semiconductor based FETs and logics are a major drawback for use in high throughput manufacturing using printing techniques. The requirement of an annealing routine within the processing steps not only makes the fabrication procedure slow and incompatible to roll-to-roll manufacturing, but it also limits the choice of flexible polymeric substrates. Therefore, alternative solutions are being sought by several research groups around the world. This chapter illustrates one of such efforts involving a 'chemical curing' method, which can eliminate surface stabilization chemically at room temperature without requiring an annealing step. Consequently, a heavily loaded oxide nanoparticulate ink is possible which can be used as the functional channel on plastic substrates and can be cured without calcination of the printed layer.

4.1. Chemical curing of oxide nanoparticles

The idea behind the concept of chemical curing is that the polymer stabilizers from the nanoparticles surface can be removed without requiring a calcination step and at the same time the printed nanoparticles would re-agglomerate and form superior interparticle contact and in general a dense and homogeneous film ideal for electronic transport. The stability of the polyelectrolyte stabilizers at certain pH is determined by the concentration of halide ions present in the ink. Hence, a below critical concentration can result in a stable ink with large shelf life, on the other hand, evaporation of the solvent after printing can cause removal of the stabilizer, agglomeration of the nanoparticles and formation of an excellent nanoparticulate film [110, 111]. However, the chemical curing concept is applied so far for metallic nanoparticles only. This concept is applied here for the first time to prepare functional oxide semiconductors for FETs. A schematic of the chemical curing and densification process of the printed oxide nanoparticulate layer is shown in **Figure 4-1**. It shows the indium oxide nanoparticle ink with added stabilizer and sintering agent (sodium chloride, NaCl). This ink is printed using a commercial ink-jet printer and dried at ambient conditions. Chemical curing occurs while drying the printed droplet. The chloride ions of NaCl during drying detach the anchoring groups of the stabilizer from the nanoparticles' surface and thus enable coalescence and sintering [110].

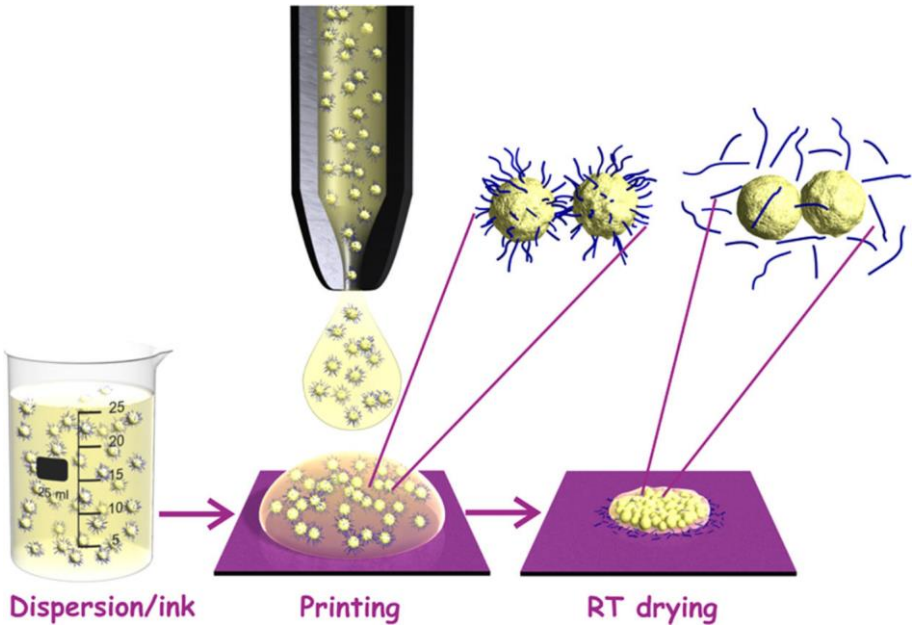

Figure 4-1 Schematic representation of the chemical curing process. Ink containing nanoparticles is printed at room temperature. During drying process ligands are removed from the particle surface.

4.1.1. Preparation of nanoparticles, inks and transistors

In_2O_3 and Cu_2O nanoparticles are used to prepare NMOS and PMOS nanoparticulate FETs. The In_2O_3 nanoparticles have been purchased from Plasmachem GmbH and used without any purification, whereas Cu_2O nanoparticles were made in the laboratory using a precipitation method [112]. To prepare Cu_2O nanoparticles, 12 g of copper nitrate salt ($Cu(NO_3)_2 \cdot 2.5H_2O$) is dissolved in water and 14 ml of triethanolamine (TEA) is added as an additive. Then the entire solution is mixed thoroughly. In parallel, 6M aqueous NaOH (17 ml) is prepared, which is added slowly drop-wise into copper nitrate solution to precipitate copper hydroxide ($Cu(OH)_2$). To this precipitate, 2 ml of 13.7 M hydrazine solution ($N_2H_4 \cdot H_2O$) is added slowly, which leads to the precipitation of Cu_2O nanoparticles. These nanoparticles are thoroughly washed as well as filtered to get rid of impurities and also dried in a vacuum oven at 60 °C for more than 12 h. Both In_2O_3 and Cu_2O NPs are characterized by XRD to find out phase and crystallite size. XRD patterns (**Figure 4-2**) confirmed that the particles are pure In_2O_3 and Cu_2O phases, respectively. Calculated crystallite size values of In_2O_3 and Cu_2O are 11, 12 nm, respectively. These particle sizes are in the range (< 100 nm) required for the preparation of stable inks. The ink-jet print head has a nozzle diameter of 20 µm and it is suitable for nanoparticles dispersions only. In addition, (dispersed) nanoparticles are less affected by gravitational forces due to large surface to volume ratio [113]. Therefore, synthesized nanoparticles can be used to prepare the stable inks.

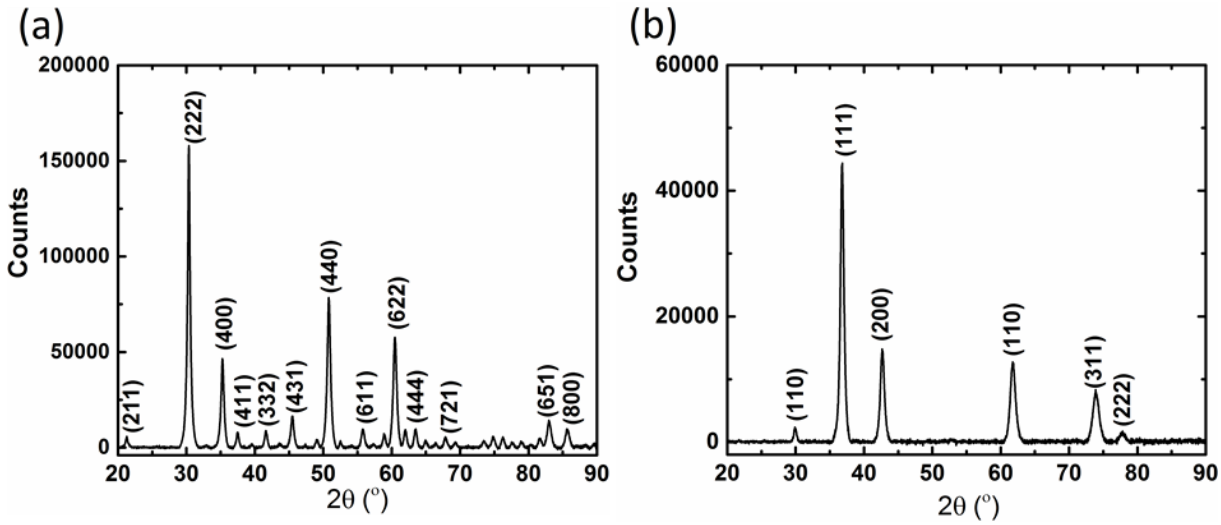

Figure 4-2 XRD patterns of (a) In_2O_3 and (b) Cu_2O. The patterns are indexed with Miller indices of the standard In_2O_3 and Cu_2O phases, respectively.

Both In_2O_3 and Cu_2O nanoparticles inks are prepared in the same procedure as follows: 1 g of nanoparticles is added to 10 ml of double distilled water, in which 150 µl of poly(acrylic acid sodium salt) (PAANa) is added as a surfactant. 10 ml of zirconia (0.2-0.3 mm diameter) pearls are added as a milling agent. A Dispermat (VMA GmbH) dissolver/mixer, which rotates at high speeds, is used to disperse the nanoparticles. The prepared mixed solution is kept under continuous stirring in the Dispermat at 8000 rpm for 90 min. Since, strong zirconia pearls are present, they can break the agglomerates during the stirring process and the surfactant protects the particles from reagglomeration. After the stirring process, the dispersion is filtered through 5, 0.45, and 0.2 µm PVDF membrane filters. After filtration, 20 mM of NaCl is added as a sintering or flocculation agent. Thus, a stable ink is obtained and used to print on FET structures. The preparation of gate insulator, in this case, is the same CSPE which is mentioned in the earlier chapter.

For device fabrication, the same in-plane FET structures on glass with ITO as electrodes and a fixed channel length of 10 µm are used for NMOS, whereas for PMOS and CMOS, silicon substrates with sputtered Cr (2 nm)/Pt (25 nm) are used. In_2O_3 and Cu_2O nanoparticulate inks are printed at RT on respective substrates for NMOS and PMOS respectively. Printed structures are allowed to dry at RT which followed by printing CSPE completes the preparation of FETs, which are characterized at ambient conditions.

4.1.2. Characterization of nanoinks

Prepared nanoinks have been investigated to find out the stability and the effect of NaCl addition. Indium oxide nanoinks using PAANa as a surfactant are found to be quite stable even for months (**Figure 4-3**). On the other hand, it is important to optimize the amount of NaCl because too much of it can easily detach the polymer ligands from nanoparticles surface and too low is insufficient to act as sintering agent. Addition of 20 mM of NaCl resulted in a quite stable ink, whereas 50 mM of NaCl showed that the ink becomes unstable and the particles agglomerate heavily and eventually settle down within an hour. However, a nanoink containing 20 mM

NaCl, reaches a critical concentration of NaCl during the drying process, which led to desorption of ligands and also particles coalesce due to strong capillary forces. The difference between the nanoink with and without NaCl can be clearly seen in the SEM images (**Figure 4-3d,e)**. SEM images of the films prepared from inks with NaCl show a substantial improvement of the densification of the nanoparticles compared to the films prepared from inks without NaCl. Hence, the addition of a critical amount of NaCl is the most important step to obtain high quality films.

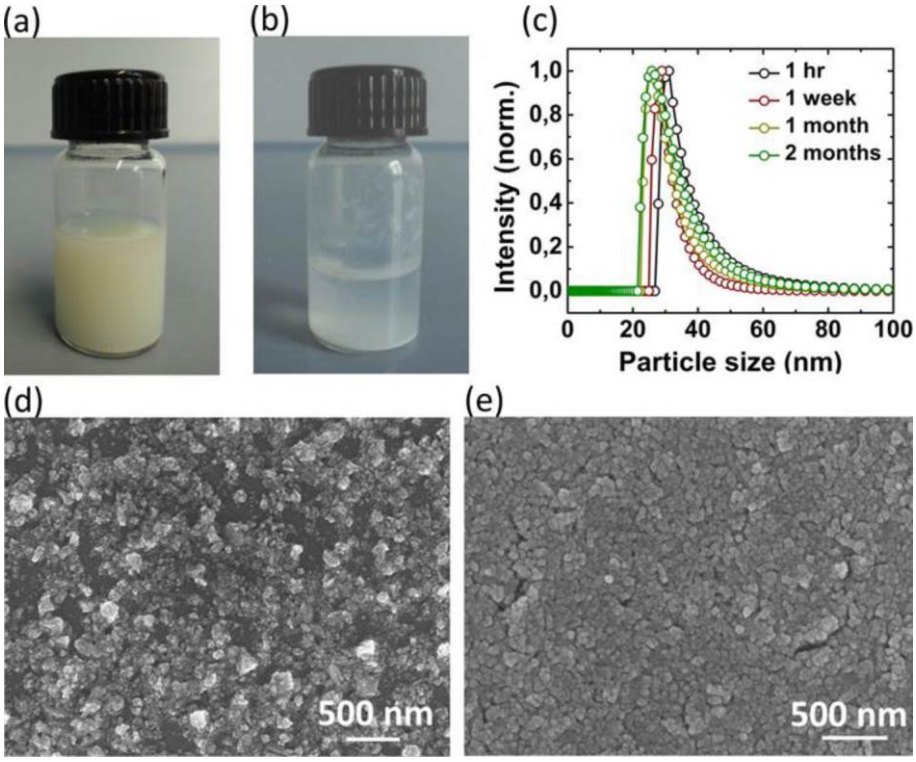

Figure 4-3 In_2O_3 nanoink with (a) 20 mM NaCl, after 2 months of ink preparation, (b) 50 mM NaCl, after 1 h of ink preparation, (c) dynamic light scattering particle size distribution with 20 mM NaCl, as a function of the elapsed time. SEM images of the printed indium oxide droplets without (d) and with (e) NaCl are also shown here.

The surface profile and thickness of the printed droplets of the In_2O_3 ink with 20 mM NaCl has been analyzed using stylus profilometer. **Figure 4-4a** shows the optical image of the printed droplet along with position of the line profiles. From the line profiles (**Figure 4-4b**), the average thickness of the printed droplet can be calculated to be approximately 180 nm. Along with the properties of the ink, the number of printed droplets influences the final thickness of the films. It is important, in case of nanoparticles, to note here that thin films (< 50 nm) have lower percolation, which will affect the electronic transport properties. On the other hand, thick films (> 300 nm) are highly conducting and require more negative voltage to switch off the device. Additionally, thick films can develop cracks during drying due to mechanical stresses. Therefore, the optimization of printed droplets is important to obtain better electrical performance. The current films are optimized to achieve high performance at RT. In addition, the printed droplet appears to be significantly homogeneous also at a macroscopic level, and no distinguishable coffee-ring pattern can be noticed. This

chemical curing phenomena is same for Cu_2O ink as well (**Figure 4-5**). Cu_2O inks with 20 mM and 50 mM are prepared and found that 20 mM is quite stable whereas 50 mM is highly unstable. Consequently, it can be presumed that 20 mM is critical to obtain stable ink. Dynamic light scattering (DLS) measurements also indicate the similar particle size distribution even after 2 months of elapsed time. It indicates that the chemical curing approach may be pertinent to almost all metal oxide systems.

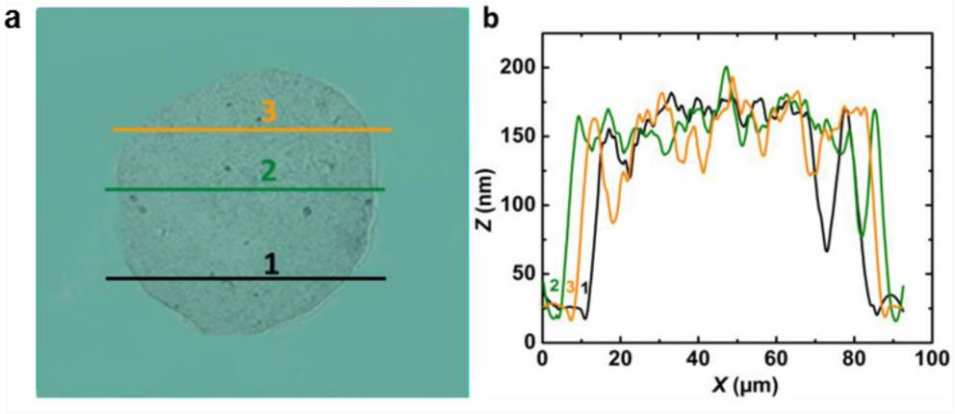

Figure 4-4 (a) Optical image of a typical, printed In_2O_3 droplet of nanoink containing 20 mM NaCl and (b) line profiles obtained at different places.

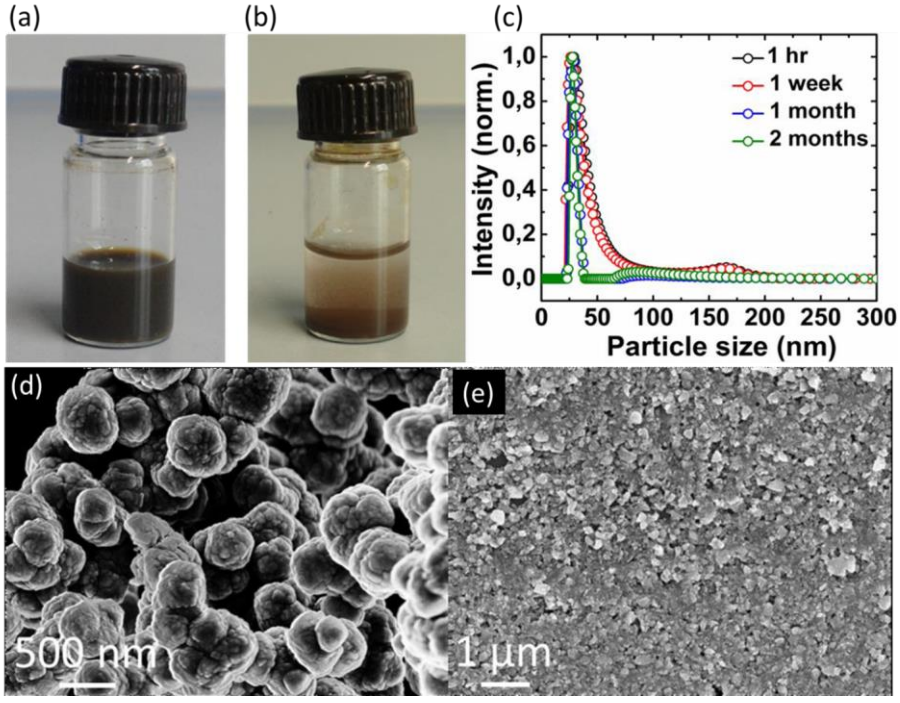

Figure 4-5 Cu_2O nanoparticle ink with (a) 20 mM NaCl loading after 2 months of ink preparation and (b) 50 mM NaCl loading after 1 h of ink preparation; (c) DLS measurements of the nanoink as a function of the elapsed time. SEM images of as-prepared Cu_2O ink (d) and the same with NaCl (e).

Poly acrylic acid (PAA) is known to be a conducting polymer, which may allow electronic transport but the removal of PAANa and densification process effect is immediately evident in sheet resistance measurements of the printed channel. Electrical resistance measurements were performed on the printed nanoparticulate transistor channel in order to evaluate the nature of electronic transport. The printed droplet is conducting even without the chemical curing agent (**Figure 4-6a**). The electronic transport across the channel in this case is possible due to the fact that the polymer stabilizer used is partially conducting. However, it shows a clear Schottky contact with the Pt electrodes (**Figure 4-6b**). In contrast, a completely Ohmic behavior and nearly 40-fold increase in the current and 20-fold increase in conductivity was noticed for a printed channel layer when 20 mM NaCl was added to the ink. This result corroborates the positives of the chemical curing process in terms of removal of the polymer stabilizer and densification of the nanoparticulate channel layer, which was then clearly reflected in an improved electronic transport. Moreover, the chemical structure of inks without and with 20 mM NaCl is studied by X-ray photoelectron spectroscopy (XPS). XPS results (**Figure 4-7**) show that carboxylic group in the C 1s spectrum is only present in the films of without NaCl ink, whereas for the films prepared with the NaCl containing ink, the carboxylic group spectrum is largely absent, which indicates the removal of ligands from nanoparticles. However, long time exposure of the films of without NaCl inks to X-rays has changes the C 1s spectra and it became similar to the ink with NaCl. On the other hand, NaCl ink has no changes for the same exposure. It means that the polymer ligands have already been removed by NaCl and additional X-ray irradiation has very little effect on the residues. In addition, the intensity of the indium peaks is higher in the films prepared from the inks containing NaCl than those without NaCl. It also indicates that the adsorbed carbon species on the indium oxide nanoparticles are removed from the surface, which improved the XPS signal of indium. Therefore, XPS studies clearly show that the NaCl has effectively removed the surfactant and improved the interparticle contacts.

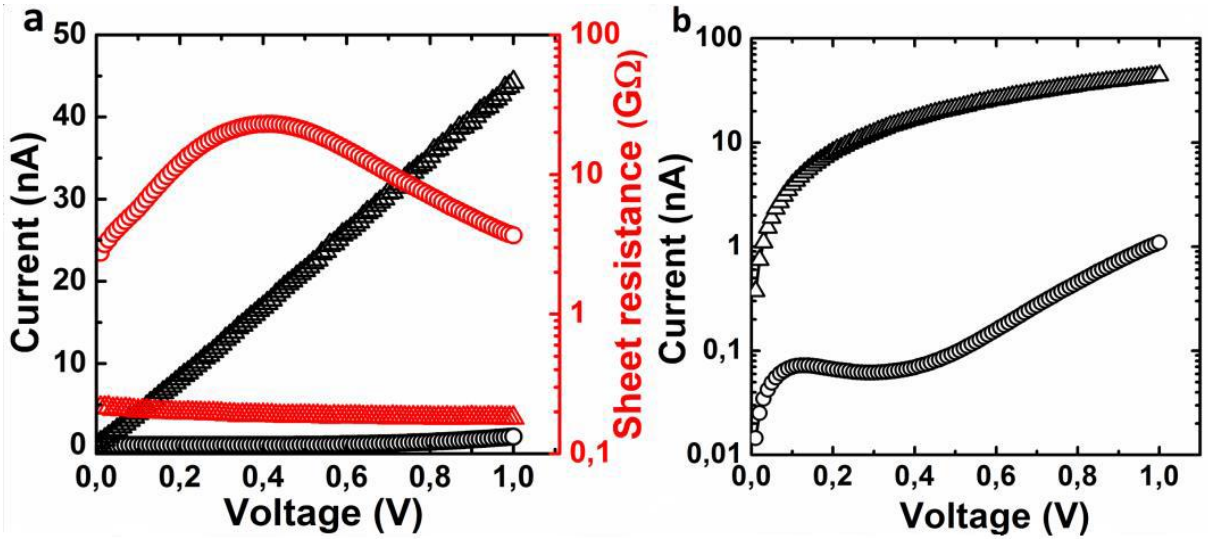

Figure 4-6 (a) Two-probe *I-V* measurement of the printed In_2O_3 nanoparticulate transistor channel without and with 20 mM NaCl in the nanoinks, the circle and the triangle correspond to nanoparticulate films without and with NaCl, respectively. The red curves correspond to the calculated sheet resistance of nanoparticulate films; (b) shows the measured two-probe currents in the logarithmic scale.

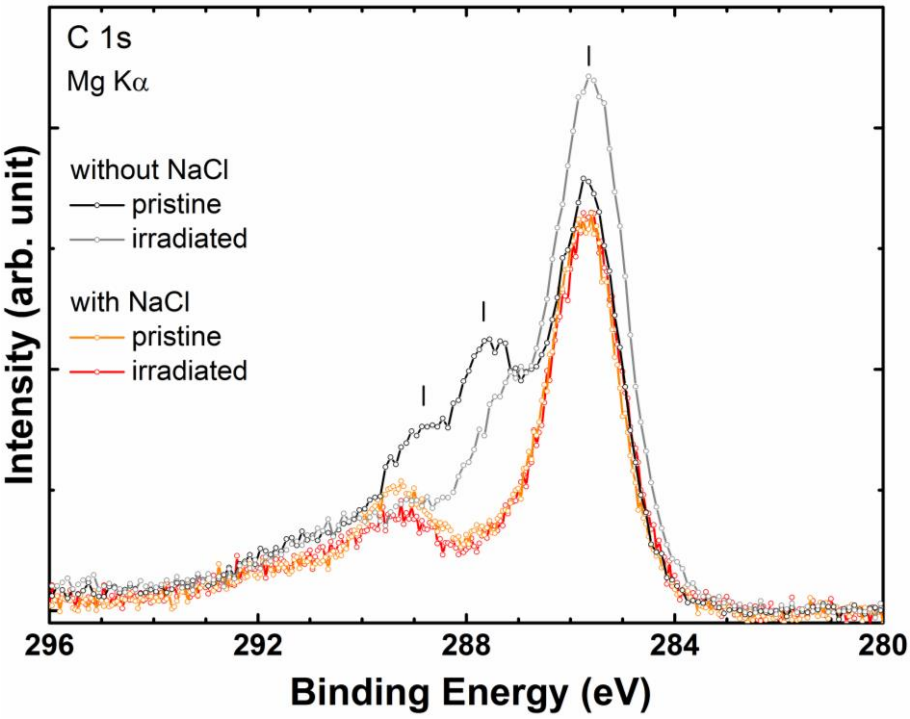

Figure 4-7 XPS spectra showing carbon (C 1s) peaks of printed indium oxide films of inks with and without NaCl additive, pristine and X-ray irradiated.

4.1.3. Transistor Characteristics of indium oxide nanoparticulate transistors

All the electrical measurements were performed in ambient air and at room temperature. Transfer and *I-V* characteristics of In_2O_3 FETs (**Figure 4-8**), processed completely at RT, show that the devices operate in accumulation mode (V_T= 0.35 V) with specific transconductance of 3.5 µS/µm, high ON/OFF ratio of 10^6 and subthreshold slope of 78 mV/decade, which is close to the theoretical limit (60 mV/decade). In addition, gate or leakage currents (I_G) are very small, i.e., in the range of picoamperes (pA). The minimization of parasitic currents from ITO electrodes, which has been mentioned in an earlier chapter as well, is the reason for this. On the other hand, the *I-V* curves show a quadratic change of drain current with the variation of the gate voltage. However, a slight negative differential resistance effect (decrease in current with increase in voltage) is observed in the *I-V* curves. Although the reasons for this effect are not clear, it might be due to the trapped ligands (acting as charge traps) between indium oxide nanoparticles. Next, in order to calculate the field effect mobility, the capacitance of the channel has to be known. One of the most accurate methods is to measure the displacement/charging current of the device itself. In order to do that, the electrolyte is printed very carefully on the channel, so that very little or almost no source-drain electrodes are in contact. The gate current is measured at different scan speeds of gate voltage and the graph (**Figure 4-8c**) predictably shows that the displacement current is almost negligible at the OFF state and rises when the transistor is ON. This behavior clearly ensures that the gate current is purely charging/displacement current (not leakage) and is also resulting from the semiconducting channel and not from the metal-like ITO electrodes. On the other hand, in the absence of any

reaction/Faradaic currents, the charging current is almost constant for different gate voltages and some reports have shown similar gate voltage dependence graphs of the charging current [114, 115]. From the current density graph, the capacitance is estimated to be 4.9 μF/cm^2 and on substituting this value in the mobility equation (equation 2.1), the obtained value is 12.5 cm^2/Vs (at V_G= 1 V) which is quite significant for completely room temperature processed, printed oxide FETs. The obtained field-effect mobility is 15 times higher than the previously reported complete room temperature processed oxide FETs [58]. This outstanding result is due to the novel chemical curing method.

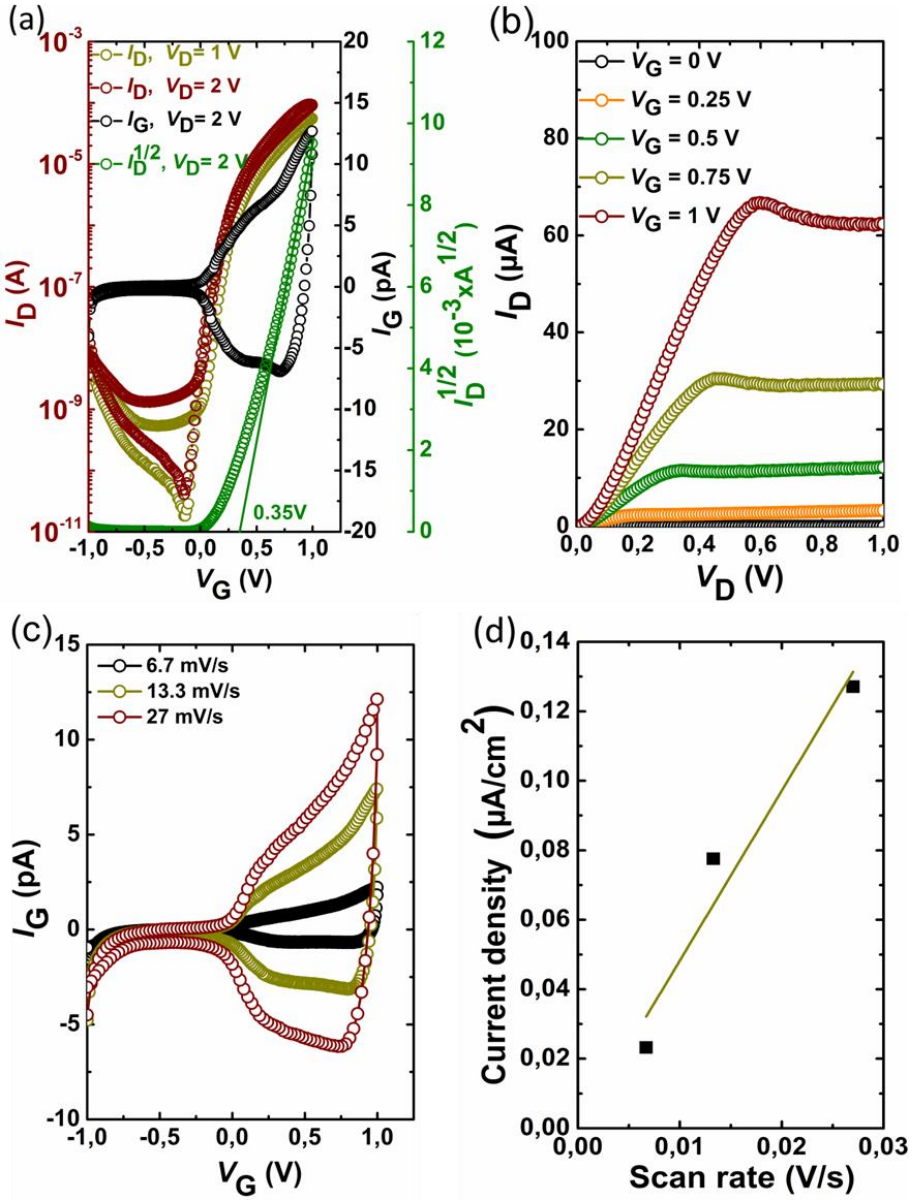

Figure 4-8 (a) Transfer, (b) *I-V* curves of In_2O_3 FET, and (c) Charging or gate current (I_G) - gate voltage (V_G) graphs of the same FET at different voltage scan speeds, (d) calculated current density (at V_G = 1 V) vs gate voltage scan speeds and the slope provides the specific capacitance of the semiconducting channel.

Field effect mobility values have also been calculated at different gate voltages in the saturation regime, using instantaneous capacitances and transconductances at each gate potential. Unsurprisingly, the mobility values did not vary for the entire range of gate voltages (**Figure 4-9**). The performance of FETs could be further

improved (μ_{FET}= 14 cm^2/Vs) by annealing at 100 °C (**Figure 4-10**). This temperature is well below the glass transition temperature of many plastic substrates, which means that these devices can still be used in flexible electronic applications. For comparison, indium oxide nanoparticulate FETs without NaCl are also prepared. The transistor characteristics are shown in **Figure 4-11**. It clearly shows that FETs with NaCl are outperforming them in terms of performance such as mobility, ON/OFF ratio, subthreshold slope, etc. All transistor parameters of In_2O_3 FETs with and without NaCl are presented in **Table 4-1**.

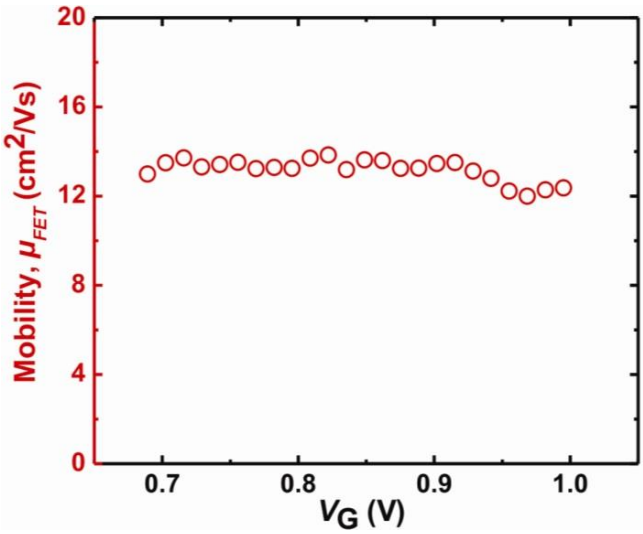

Figure 4-9 Calculated field-effect mobility values of indium oxide FET (with NaCl) at different gate voltages in the saturation regime.

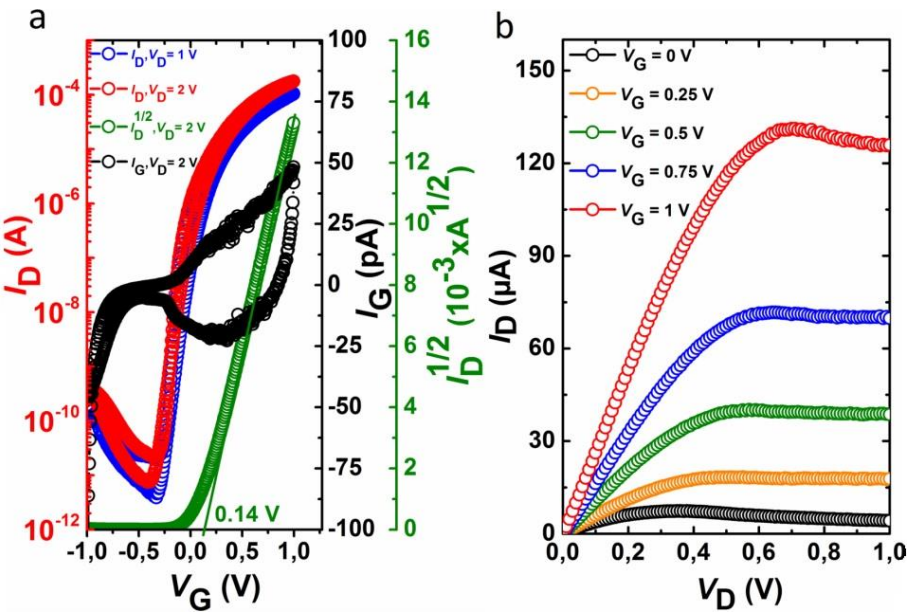

Figure 4-10 (a) Transfer and (b) *I-V* characteristics of a representative FET device prepared from In_2O_3 nanoink with 20 mM NaCl and the printed channel has been annealed at 100 °C after printing.

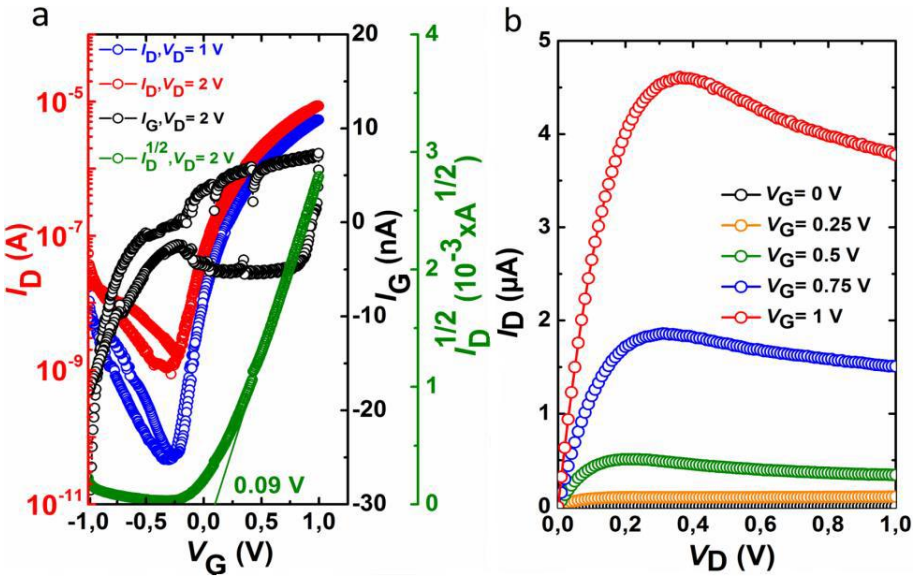

Figure 4-11 (a) Transfer and (b) *I-V* characteristics of a representative FET device prepared from In_2O_3 nanoink without NaCl.

Nanoink FETs	*SS* (mV/decade)	G_m (μS/μm)	μ_{FET} (cm^2/(Vs))
Without NaCl, RT	140	0.5	0.95
With NaCl, RT	78	3.5	12.5
With NaCl, 100 °C	73	5.3	14

Table 4-1 The transistor characteristics table of indium oxide nanoparticulate FETs. The table shows the subthreshold slope, the transconductance and the field-effect mobility of transistors of uncured (without NaCl), chemically cured (with NaCl), cured as well as heated at 100 °C.

4.2. Complementary metal oxide semiconductor inverter at room temperature

To realize RT processed all oxide CMOS inverters, p-type Cu_2O nanoparticles based PMOS transistors are fabricated first. Identical to In_2O_3 nanoink, the Cu_2O nanoink has also been prepared using PAANa and 20 mM NaCl as surfactant and sintering agent, respectively. Printed Cu_2O films show relatively granular features compared to In_2O_3 films, due to large agglomerates in the as-prepared powder. The Cu_2O nanoparticles did not rupture even during ink preparation. These large agglomerates affected the film quality adversely, which in turn influenced the transistor characteristics (**Figure 4-12**) and relatively poorer performance than the NMOS FETs are obtained. Nevertheless, the prepared CMOS inverter, combining the oxide NMOS and PMOS inks, demonstrates decent signal gain and dynamic performances. Once again, the passive structures are lithographically defined with a fixed channel length of 2 and 10 μm for PMOS and NMOS respectively. The width to length (W/L) ratios of PMOS and NMOS are approximately 10 and 1, respectively. CMOS inverter characteristics are shown in **Figure 4-13**. The signal/voltage gain curves are observed for different drain

voltages (0.5-1.5 V) and there is a shift in the transition voltage as well as signal gain, which is due to change in the performances of both the FETs at particular drain voltages. Switching threshold voltages (V_{IN} = V_{OUT}) are close to the ideal (V_{DD}/2) [116] ones at low drain voltages, however, it shifted to lower values at higher drain voltages which might be due to the unmatched performance of both the FETs. On the other hand, the achieved maximum signal gain (18) is significantly high for a RT processed CMOS, in fact it is better than sputtered oxide CMOS [108]. In addition to high voltage gain, very low static power consumption (< 1 nW) is also observed. The other figure of merit for inverters is noise margin, which in the present case varied with voltage. For example at low voltages NM_H and NM_L are close, whereas at higher voltages, the difference is also wider but the forbidden region is on average of 0.2 V (**Figure 4-14**). A complete list of characteristic values is shown in **Table 4.2**. This table indicates that the voltage gain of an inverter is a function of V_{DD}. Out of several factors, mobility and threshold voltages are the most important factors that determine the voltage gain [117]. It means that, in the present case, both mobility and threshold voltages of FETs are relatively matching at higher V_{DD} and thereby voltage gain is higher at higher V_{DD}. Therefore, electrolyte-gated devices require a voltage of at least 1 V to achieve a gain of ≥ 10. However, most of the thin film batteries can produce 1 V, so the present devices are compatible with thin film battery applications and thereby portable electronic applications.

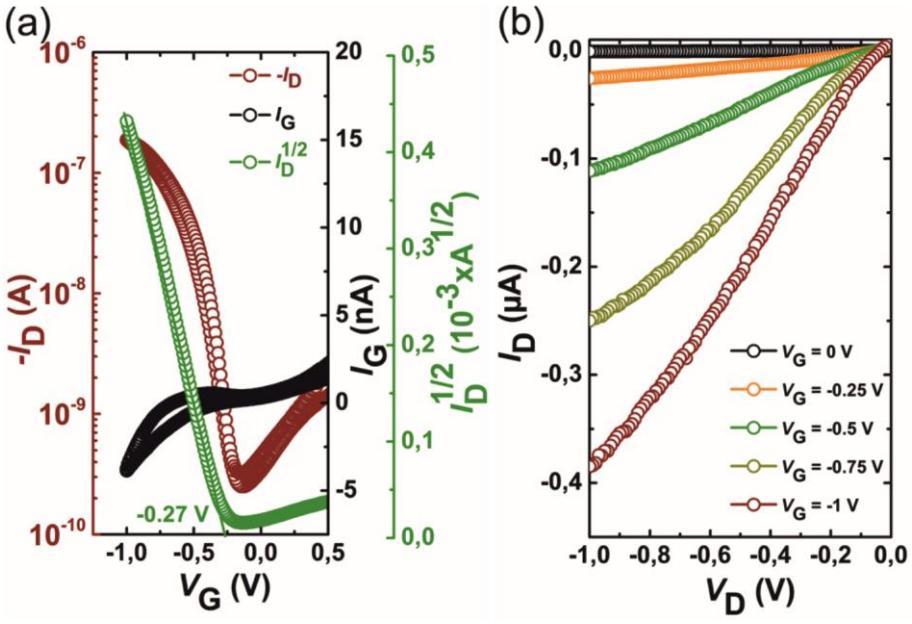

Figure 4-12 (a) Transfer and (b) *I-V* curves of Cu_2O FET. The Cu_2O nanoparticulate channel layer has been fabricated from 20 mM NaCl containing, PAANa stabilized Cu_2O nanoink.

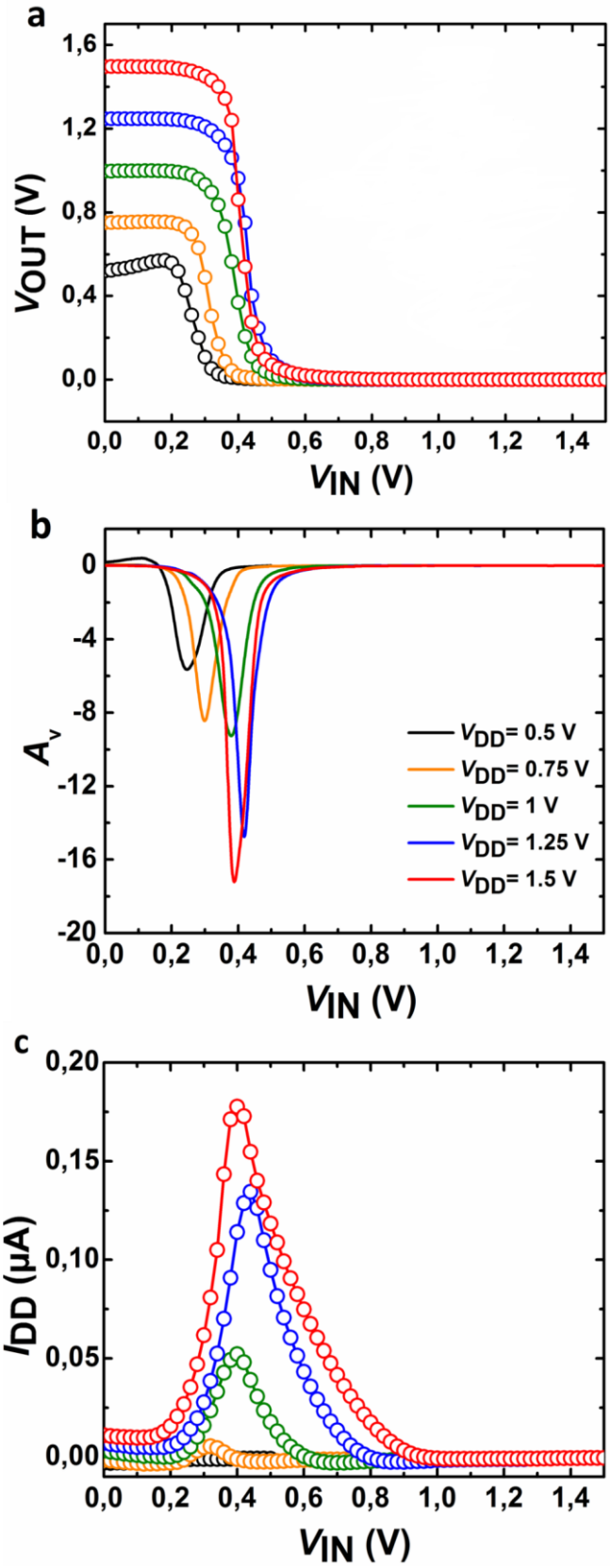

Figure 4-13 CMOS inverter (prepared by chemical curing at room temperature) graphs showing (a) transfer, (b) voltage gain (Av) and (c) drive current (I_{DD}) curves. Graphs show the variation of voltage gain as well as drive currents with V_{DD}. The CMOS inverter is comprised of In_2O_3 (n-type) and Cu_2O (p-type) FETs.

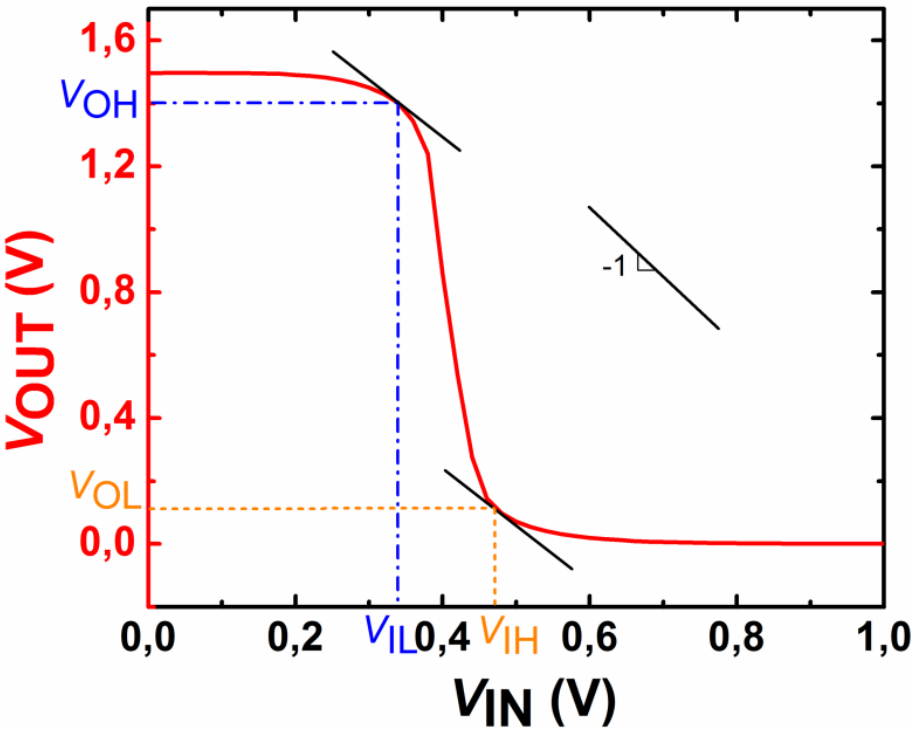

Figure 4-14 An exemplary noise margins calculation is shown. The CMOS inverter transfer curve at a supply voltage of 1.5 V is used to calculate noise margins.

V_{DD} (V)	Switching threshold voltage (V)	Voltage gain	NM_H (V)	NM_L (V)	Forbidden region (V)
0.5	0.25	6	0.21	0.18	0.15
0.75	0.3	8	0.34	0.21	0.17
1.0	0.28	10	0.49	0.23	0.23
1.25	0.42	15	0.68	0.25	0.25
1.5	0.39	18	0.93	0.23	0.13

Table 4-2 A table showing noise margin characteristics (the source or drive voltage, the switching threshold voltage, the voltage gain, the high noise margin, the low noise margin and the forbidden regions) of the room temperature processed CMOS inverter.

In summary, chemical curing of nanoparticles, which doesn't involve any additional process step, is used to demonstrate completely RT processed oxide FETs that include NMOS, PMOS and also logics, i.e. a CMOS inverter. In the chemical curing process, a sintering agent (NaCl) is used to detach the polymer ligands (PAANa) from nanoparticles surface. Coalesce of particles happens due to strong capillary forces. The amount of NaCl is determined to be critical, because it affected the stability of the ink, morphology of the films, and also sheet resistance of the channel. The performance of the indium oxide FETs is significantly higher (μ_{FET}=

12.5 cm^2/Vs) for the inks, which contain NaCl when compared to the FETs that made of inks without NaCl. Using the same procedure, Cu_2O FETs have also been prepared and combining these two, a CMOS inverter has also been fabricated, which showed very high voltage gain of 18 at RT. This result is outstanding, in fact better than sputtered oxide CMOS. This achievement surmounted long standing challenge of high performance oxide FETs at RT. However, a good quality PMOS, can still improve the gain and also noise margins of CMOS. Nevertheless, achieved results indicate the novelty of the chemical curing for oxide FETs and logics, which can open applications for flexible electronics.

5. Photonic Curing of Printed Metal Oxide Field-effect Transistors

Similar to the last chapter, here an attractive approach for low temperature processing of oxide nanoparticles as well as oxide precursor based FETs is presented based on photonic curing of the semiconductor layer. Two different approaches have been chosen: (a) a homogeneous irradiation of the complete substrate with functional devices to a high energy UV-visible radiation, and (b) local heating with monochromatic UV-lasers.

5.1. Photonic curing techniques for oxide transistors

Oxide FETs have shown excellent FET characteristics that are equally good and often superior to organic FETs. However, for oxide electronics process temperature is a longtime issue of concern. The crystallization or formation temperature of oxides is typically much higher than for organics materials, which limits the choice of inexpensive polymer substrates [118-120]. In order to reduce the formation temperature of metal oxides, different methods such as "sol gel on chip" (annealing in controlled aqueous environment enhances hydrolysis reaction) [83], "combustion synthesis" (combination of oxidizer and fuel reduces the activation energy barrier) [73], etc., have been adopted and reported in the past. However, in both cases, the critical device parameter, i.e. the field effect mobility value suffers considerably when the process temperature is lowered to 200 °C or below. In addition, for combustion synthesis, the addition of fuel may raise the precursor temperature locally, which is well above the hot-plate temperature, and thus may damage the polymer substrate that can be used.

In this context, an alternative approach, namely the photonic curing techniques (light with ultra-violet (UV) range wavelength) can be used to cure or sinter the films. In this case, the photons with very high energy interact with oxide nanoparticles (or precursors) to sinter the nanoparticles and remove the unwanted semi-insulating organic species (used for stabilizing the particles) from the surface or to crystallize the desired metal oxide phase from the metal salt based precursors. The advantages of these techniques are high energy density, high throughput, but most importantly, the selection of the substrate is possible, which is transparent to the chosen wavelength, resulting in a negligible energy received by the substrate. Photonic curing techniques have been investigated earlier for metals [121, 122], oxides [123], semiconductors [124], etc. Yang et al. prepared indium gallium zinc oxide (IGZO) films by spin coating the nanoparticle ink on a glass substrate and sintered them using Nd:YAG laser (λ = 355 nm). The achieved mobility was 7.65 $cm^2V^{-1}s^{-1}$ [125]. Pan et al. reported krypton fluoride (KrF) excimer laser (λ = 248 nm) sintered ZnO FETs but the mobility value was only 0.1 $cm^2V^{-1}s^{-1}$ [126]. Park et al. sintered indium tin oxide (ITO) nanoparticles using KrF excimer laser (λ = 248 nm) and this showed 1000 fold increase in the conductivity [127] but no FET has been reported. Kim et al. reported UV irradiated (mercury lamp with wavelengths of 253.7 and 184.9 nm) oxide FETs prepared by spin coating the precursors on glass and also on polymer substrates with a mobility of 14 and 7 $cm^2V^{-1}s^{-1}$, respectively [84].

However, there was unintentional heating (150 °C) of the substrates due to which it has not been possible to use inexpensive plastic substrate such as PEN.

In order to circumvent many of these issues, high energy UV-visible light pulses for extremely short times (few tens of seconds) have been used to cure the precursor and nanoparticles films on glass and PEN substrates, respectively. In parallel, continuous wave helium (He)-cadmium (Cd) laser has been used to cure similar batches of films with moderate scan speeds. As the exposure time is very short, the substrate receives a very low amount of energy and the associated temperature rise is negligible. Furthermore, high performance FETs on polymer substrates have obtained by combing high energy UV-visible light pulses or monochromatic UV-laser cured channel with CSPE-gating.

5.2. Preparation of high energy UV-visible light and monochromatic UV-laser cured transistors

In the present study, indium oxide is used as the semiconductor material to form the channel of the FETs. Two different approaches are used to prepare the semiconducting channel, i.e. metal oxide precursor and oxide nanoparticles. In the precursor route, indium salts are dissolved in a suitable solvent, which is then printed onto a substrate and cured with high energy UV-visible light pulses and monochromatic UV-lasers. In order to prepare the ink for the precursor route, indium nitrate hydrate is dissolved in water and glycerol mixture (4:1 volume ratio) and filtered through 0.2 µm PVDF membrane. The filtered precursor is printed using Dimatix DMP 2831 ink-jet printer on glass substrate which has lithographically patterned passive structures (ITO electrodes). Printing of the precursors has been performed with a substrate temperature of 50 °C to evaporate the ink solvent quickly and thereby to prevent unwanted spreading of the films. The printed film is then dried at 100 °C for 2-3 min. Next, the dried films are cured either with high energy UV pulses or with the monochromatic UV-laser. In the NP approach, indium oxide nanoparticles are dispersed in water using PAANa as a surfactant and then the printed films are cured with UV-visible light pulses and monochromatic UV-laser. The indium oxide nanoparticles' ink preparation details are mentioned in the previous chapter. The prepared NP ink is printed on PEN substrates and dried at ambient conditions before the application of continuous UV-visible light pulses and monochromatic UV-laser curing.

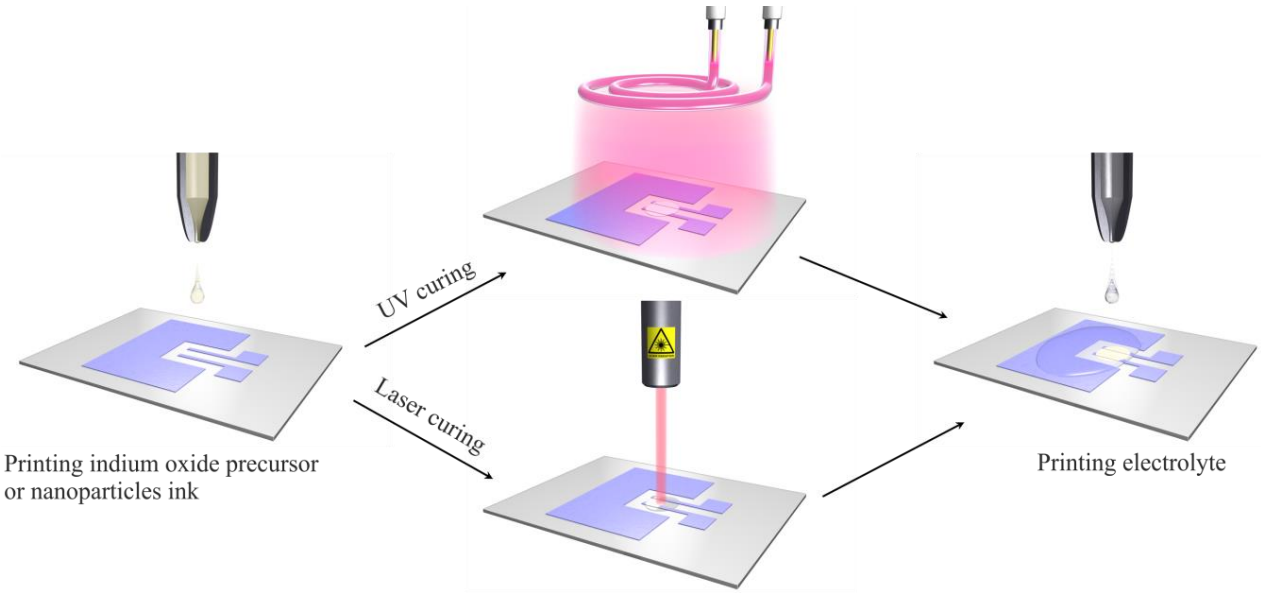

Figure 5-1 Schematic of UV-visible and UV-laser curing of indium oxide transistors. Processing steps include printing of the semiconductor, followed by photonic curing and printing of electrolyte.

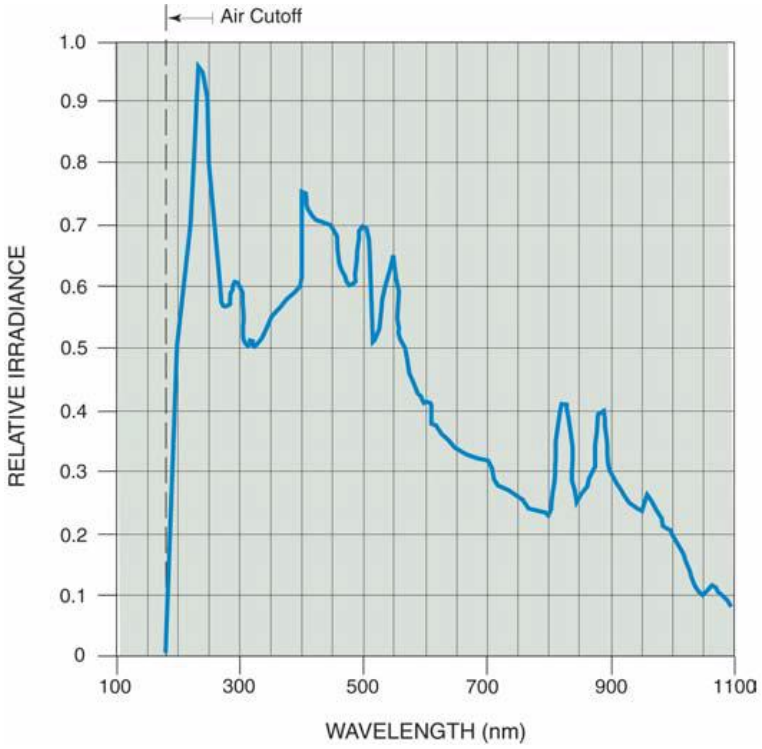

Figure 5-2 Wavelength and corresponding intensity spectrum of the pulsed UV-visible light source (adopted from www.polytec.com)

A schematic of the preparation of FETs using different photonic curing techniques is shown in **Figure 5-1**. Indium oxide precursors or In_2O_3 nanoparticles are printed onto a lithographically patterned FET structure where indium tin oxide (ITO) is used as the electrode material in order to obtain Ohmic contacts. After the drying process, the printed channel layers are cured using either a broad spectrum high energy UV-visible light

source or a monochromatic UV-laser, which is followed by the printing of composite solid polymer electrolyte gate dielectric. The major differences between the broad spectrum high energy UV-visible light source and the monochromatic UV-laser are exposure area and energy density. In case of the UV-visible light source, a very high energy UV-visible light (the wavelength and corresponding intensity of the lamp is shown in **Figure 5-2**) is used to radiate the whole substrate. Along with UV, visible light radiation is also present in the spectra of this lamp. Hence, it is named as UV-visible light. In case of UV-laser, only the selected area on the substrate, where the semiconductor layer lies, is exposed to moderate energy monochromatic UV-laser light. The advantages of broad spectrum UV-pulses are high energy density for short period, large area exposure, high speed, etc., and the disadvantages are unavoidable substrate heating, requirement of protection chamber, degradation of lamp life with time etc. In contrast, the advantages of laser curing technique are selectivity, as well as highly localized exposure, moderate energy density, while the disadvantages are low speed, small areas etc. However, both UV and laser techniques are complementary to each other and can be used based on the requirements and necessity of the specific application.

5.2.1. High energy broad spectrum UV-visible light curing

UV pulse generator (Sinteron 2000, Xenon corp.) with a lamp of spectral cut-off wavelength of 190 nm is used for UV-visible light curing. The glass substrate with printed structures is placed on a sample holder (thickness is around 2.5 mm), which is placed at a distance of approximately 25 mm (optimized distance) from the UV-visible curing lamp. High (2070 J) and low energy (500 J) UV-visible light -pulses are applied on the glass and PEN substrates, respectively, for different pulse times (30-240 s) with a fixed frequency of 1.8 Hz.

5.2.2. Monochromatic UV-laser curing

A focused continuous wave He-Cd laser (wavelength of 325 nm) with a spot size of 10 µm is used for the monochromatic wavelength UV-laser curing of the printed films. High (53.5 mW, 500 µm/s) and low (6 mW, 100 µm/s) laser power and different scan speeds have been used for glass and PEN substrates, respectively.

5.2.3. Characterization techniques

Structural characterization for phase, morphology and roughness has been carried out using XRD, SEM and AFM, respectively. X-ray Photoelectron Spectroscopy (XPS) measurements have been performed using a K-Alpha+ XPS spectrometer (Thermo Fisher Scientific, East Grinstead, UK). Data acquisition and processing was done by using the Thermo Avantage software [128]. All samples have been analyzed using a microfocused, monochromated Al Kα X-ray source (30-400 µm spot size). The spectra were then fitted with one or more Voigt profiles (binding energy uncertainty: ± 0.2 eV). The analyzer transmission function, Scofield sensitivity factors

[129], and effective attenuation lengths (EALs) for photoelectrons have been applied for quantification. EALs were calculated using the standard TPP-2M formalism [130]. All spectra are referenced to the C1s peak of hydrocarbon at 285.0 eV binding energy controlled by means of the well-known photoelectron peaks of metallic Cu, Ag, and Au.

5.3. Structural characterization of UV-visible light and UV-laser cured indium oxide precursors as well as nanoparticles

In this section, XRD, SEM, AFM, XPS analyses of indium oxide precursor as well as nanoparticulate films, which cured by UV-visible light and UV-laser, are presented.

5.3.1. UV-visible light curing of precursors

For structural characterization, a similar batch of cleaned glass slides with a size of 1 cm^2 have been used and a very small amount of precursor solution was cast on these substrates, then dried at 100 °C. High energy UV-visible light pulses (2070 J) were applied on these dried films for different time periods (30-90 s). Grazing incidence XRD studies performed for these cured films are shown in **Figure 5-3**. Indium oxide phase formation started as early as 60 s exposure to UV-pulses and the crystallinity improved further with increasing number of pulses, up to 90 s. Calculated crystallite sizes (using the Debye-Scherrer equation) of the cured films for 60 and 90 s are 12 and 12.3 nm, respectively. Small crystallite sizes are due to the fact that high boiling point glycerol (290 °C) prevents the growth of crystals [131]. However, a further optimization of the energy density of UV-visible light may improve the crystallinity as well as crystallite size. The formation of indium oxide from nitrate precursor can be explained by sol-gel reaction, which is driven by the high energy photons in the present case. Dissolved indium nitrate ions form hydroxide, which then condensates to form metal-oxygen-metal bonds due to photochemical activation [84].

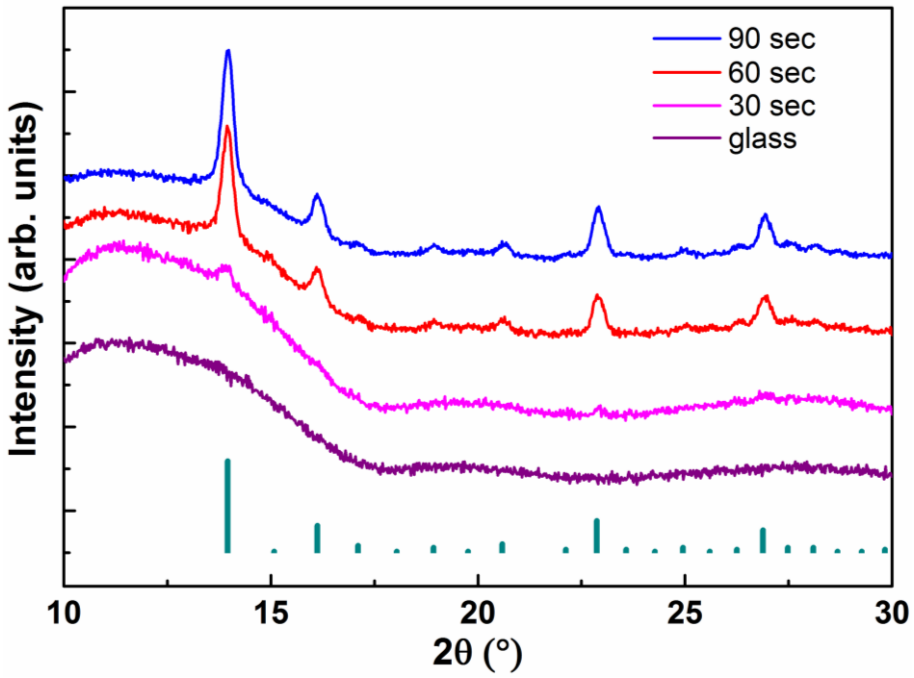

Figure 5-3 XRD patterns (including reference patterns of indium oxide, i.e. vertical green lines at the bottom) of UV-visible light cured indium oxide precursor films for different pulse times (30-90 s) on a glass substrate.

SEM and AFM analyses have been carried out to characterize morphology and surface roughness of the films. SEM and AFM images (**Figure 5-4**) show that the films are homogeneous with solid network of particles and also very smooth (RMS roughness of only 0.5 nm). The surface roughness and the section analyses of AFM micrographs of the same sample are shown in **Figure 5-5**. These images indicate that the films are very smooth and the roughness amplitude is less than 1.5 nm. The reason for such a low roughness in the films is the addition of high boiling point glycerol. It indicates that the solvents along with salts play a major role in determining the film quality. The prepared films are smooth and suitable not only for electrolyte but also for other conventional oxide dielectrics. A smooth film can form a good interface with the dielectric and decreases interface scattering of charge carriers. This eventually improves the performance of the devices.

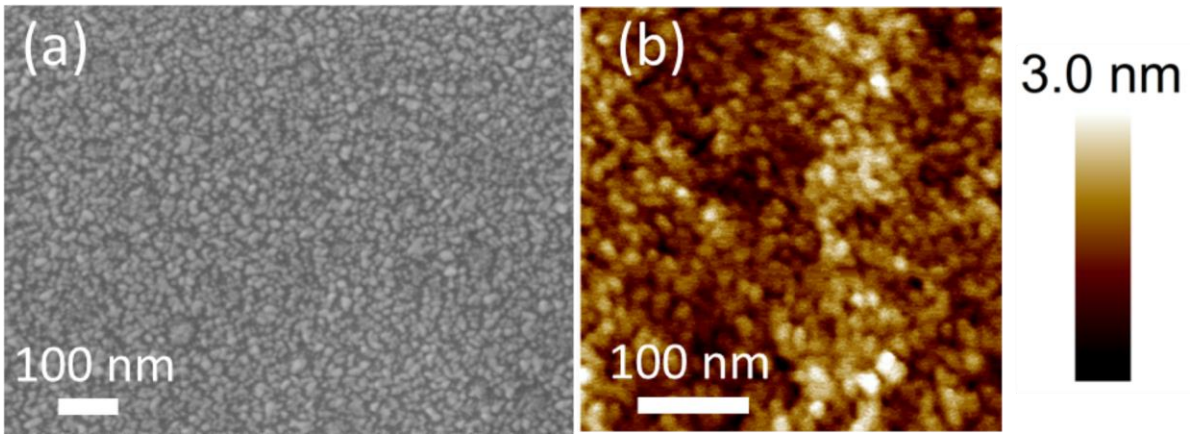

Figure 5-4 (a) SEM and (b) AFM images of UV-visible light cured (pulses for 90 s) indium oxide precursor films.

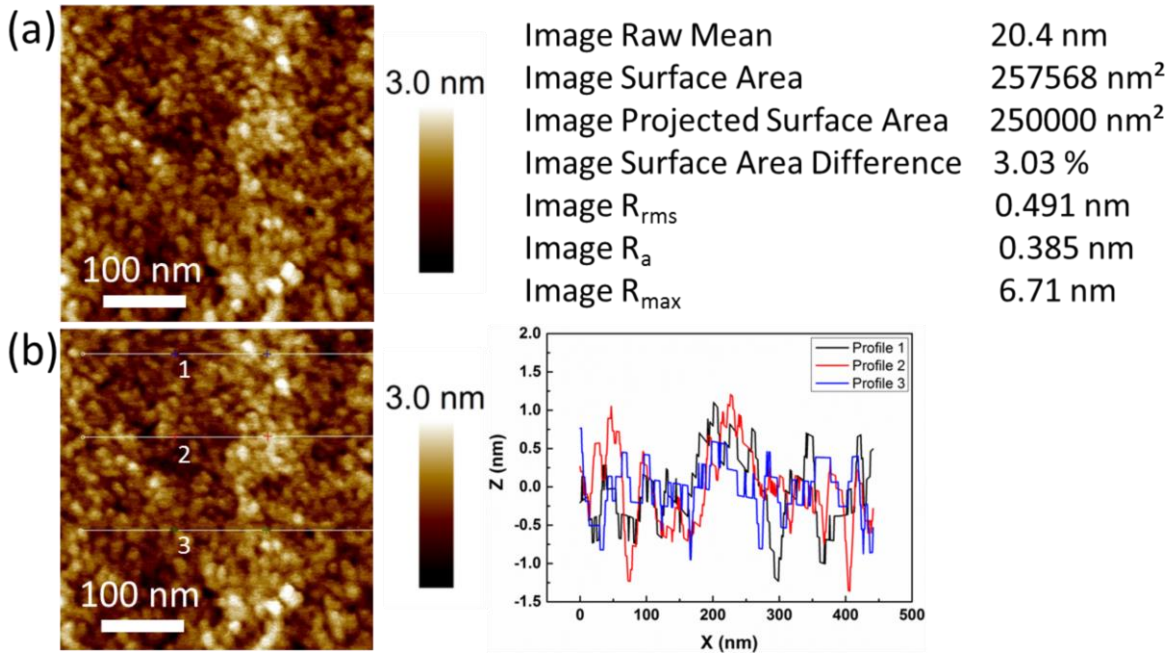

Figure 5-5 (a) Surface roughness and (b) section analysis of AFM micrographs of UV-visible light cured (pulses for 90 s) indium oxide precursor films.

5.3.2. Monochromatic UV-laser curing of precursors

He-Cd continuous wave laser has been used to cure the casted/printed precursor films. XRD patterns of precursor films before and after curing are shown in **Figure 5-6**. It is clear that the indium oxide is formed without any secondary phase after monochromatic UV-laser curing of the films. Calculated crystallite size is 19.4 nm. It is observed that the crystallite size of UV-laser cured films is larger than UV-visible cured films. This might be due to the high energy density of UV-laser. Next, the SEM and AFM analyses have been performed. SEM and AFM images (**Figure 5-7**) show that the monochromatic UV-laser cured films are continuous without any cracks and also smooth (RMS surface roughness of only 2 nm). AFM images indicate that the roughness of the films is higher than UV-visible light cured precursors. Surface roughness and section analysis images are shown in **Figure 5-8**. Section analysis image shows the distribution of particles and also the particle sizes are close to the calculated XRD crystallite size value. Roughness analysis image indicate that the maximum amplitude of surface roughness is greater than 6 nm. Therefore, such rough films may have somewhat affected the electrical performance.

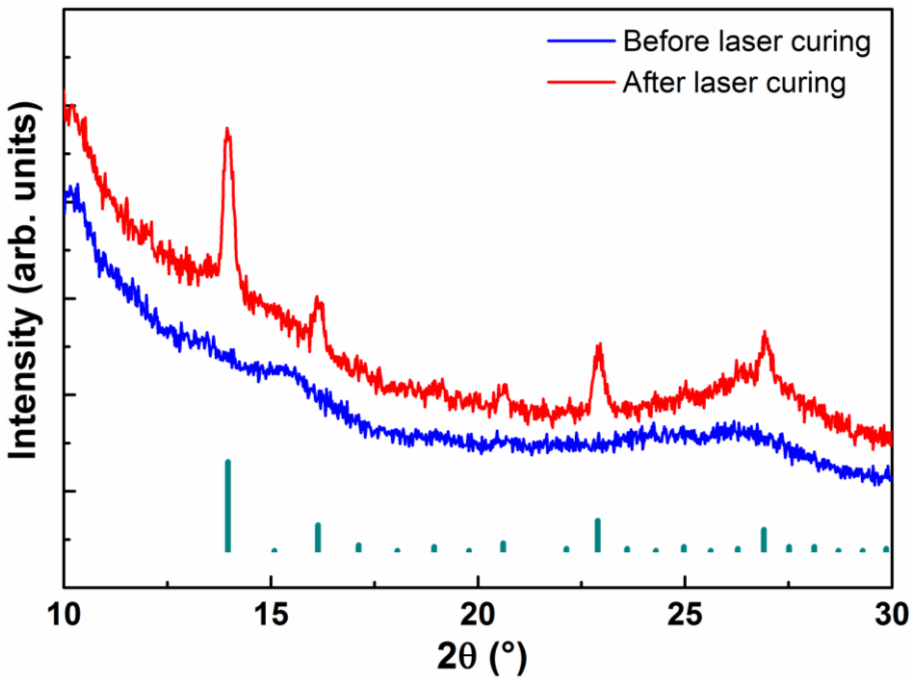

Figure 5-6 XRD patterns of UV-laser cured (with a laser power of 53.5 mW) indium oxide precursor films on glass substrates. These patterns include standard reference patterns of indium oxide (vertical green lines).

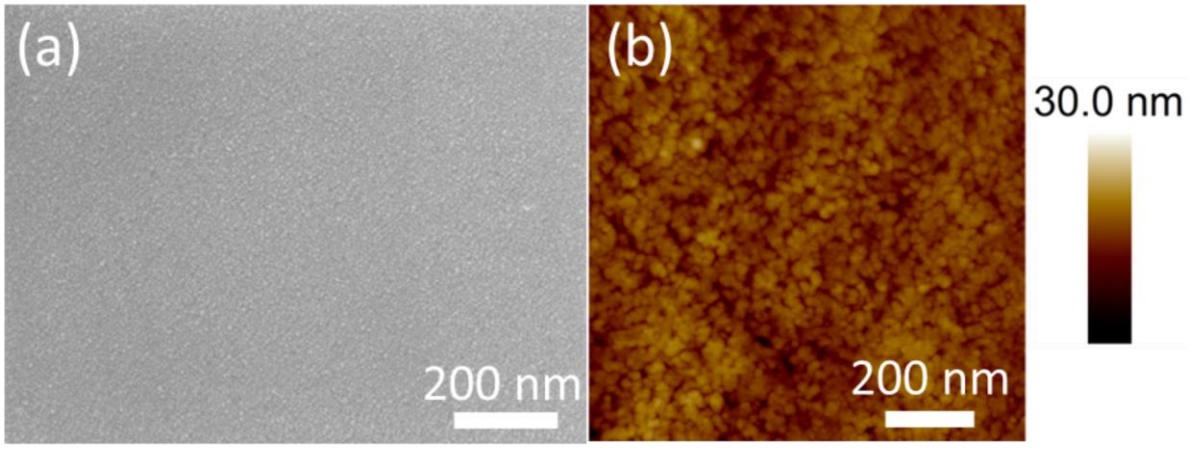

Figure 5-7 (a) SEM and (b) AFM images of monochromatic UV-laser cured (with a laser power of 53.5 mW) indium oxide precursor films.

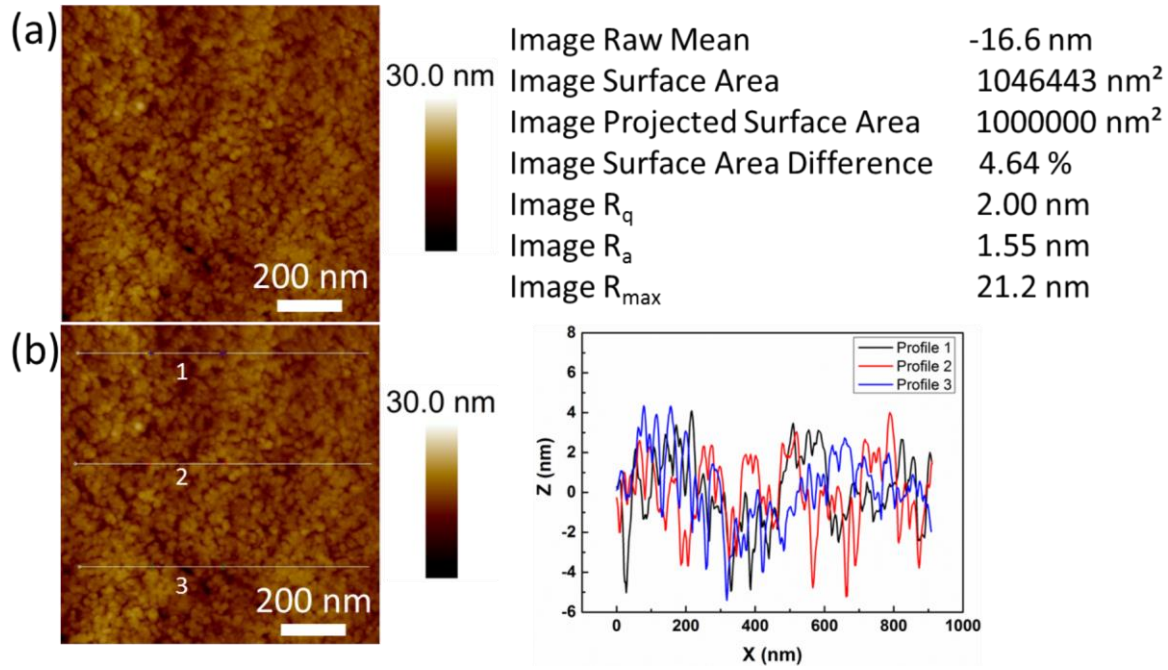

Figure 5-8 (a) Surface roughness and (b) section analysis of AFM micrographs of monochromatic UV-laser cured (with a laser power of 53.5 mW) indium oxide precursor films.

5.3.3. UV-visible light curing of nanoparticles

Printed In_2O_3 nanoparticulate films on PEN substrates have also been cured using UV-visible light radiation. Once again, these films have been characterized by SEM. SEM images show that the printed indium oxide nanoparticulate films have moderate interparticle contact and low porosity. SEM images (**Figure 5-9**) also indicate that there is no significant change in the bulk morphology or densification of the nanoparticles before and after the UV-visible light exposure.

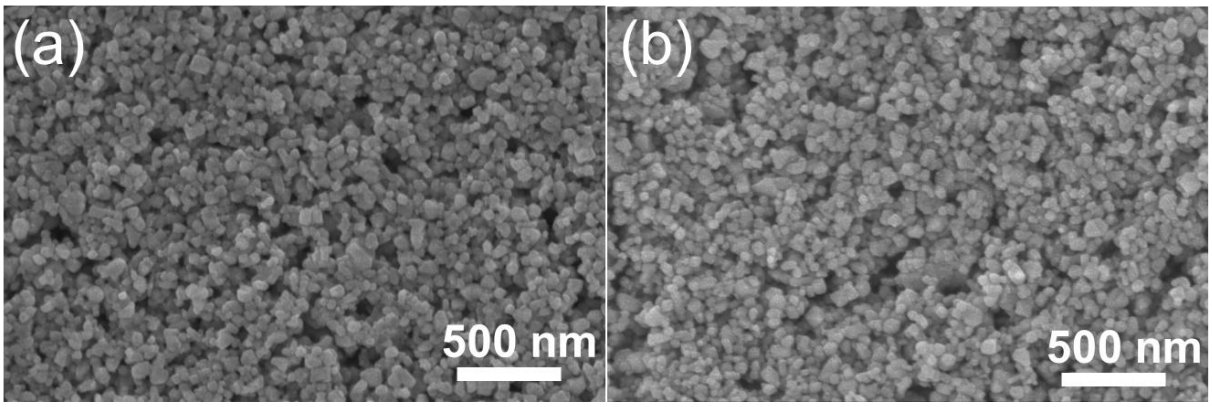

Figure 5-9 SEM images of indium oxide nanoparticulate films (a) before and (b) after UV-visible light curing (pulses for 10 s).

In order to analyze the composition of these films, XPS studies have been carried out on the array of printed indium oxide NP droplets which had been dried at room temperature. For the as prepared films, the carbon (C 1s) spectrum in **Figure 5-10a** shows the three PAANa components at 285.0 eV, 286.7 eV, and 288.4 eV, which are assigned to C-C/C-H, C-O, and COONa groups, respectively [132]. Due to the negative charge of the COO group the respective peak is slightly shifted to lower binding energy compared to COOC groups [133]. The corresponding O 1s peaks in **Figure 5-11b** appear at 531.8 eV (O=C-O) and 532.8 eV (C-O). However, the peak at 531.8 eV is overlapped by contributions from indium oxide and the native silicon oxide of the substrate, respectively, which cannot be differentiated. In addition, In_2O_3 clearly can be identified by the In $3d_{5/2}$ peak at 444.5eV [134] in **Figure 5-11a**. All findings are in a good agreement with literature and clearly evidence the PAANa capping agent on the NPs. The intensities of peak at 286.7 eV and 288.4 eV reduced after sample curing as compared to as-prepared sample. Furthermore, the comparison of the concentration of the different carbon groups normalized to the Si-O content in **Figure 5-10b** directly proves the decrease of the PAANa after UV-visible light curing when compared to as-prepared films. In addition, the intensity of indium peak improved and sodium peaks decreased when compared to uncured sample. Therefore, XPS results indicate that the UV-visible light curing decomposed (partially though) the capping agent and improved the interparticle contact. This in turn ensured better electronic transport when compared to uncured films.

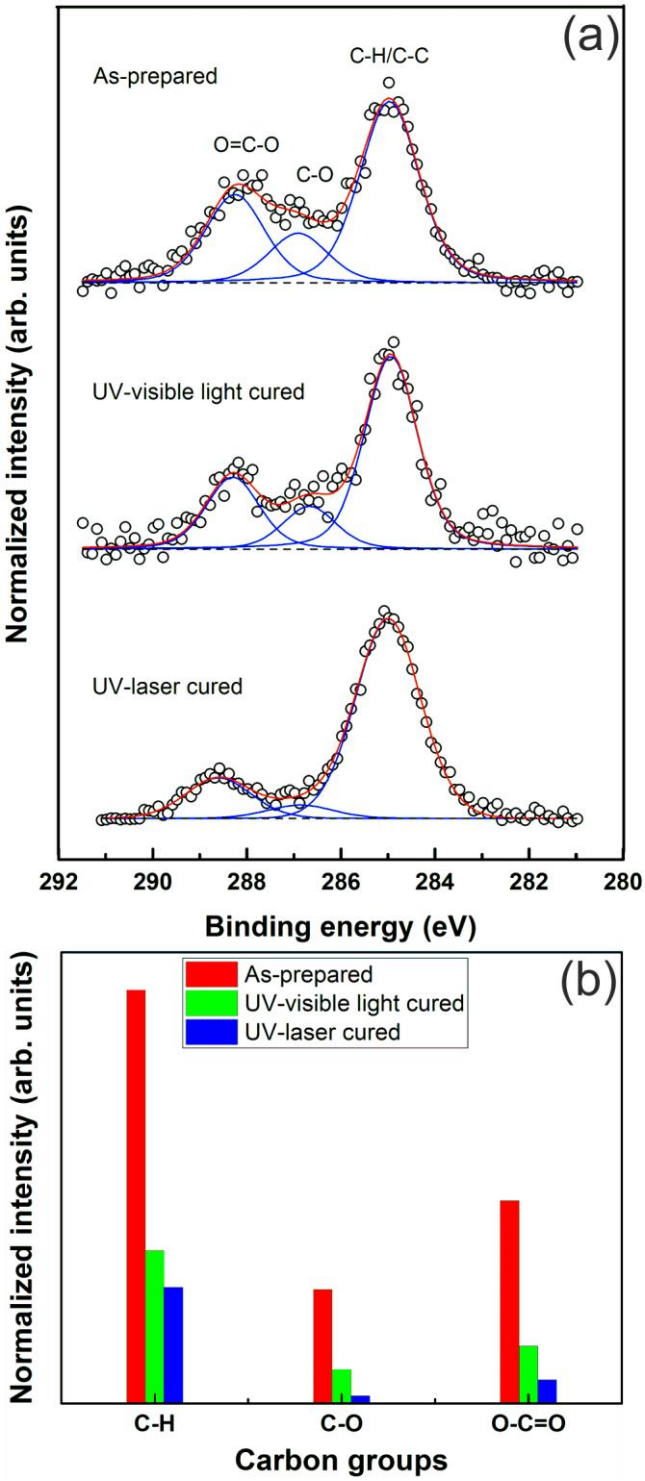

Figure 5-10 XPS results of as-prepared and photonic cured indium oxide nanoparticulate films. (a) Comparison of the carbon (C 1s) spectra normalized to maximum intensity and (b) comparison of the respective atomic concentration ratios normalized to the Si-O content. In the graph (5-10a), measured data (black color circles), fitted data (red color lines) and deconvolution of carbon group peaks (blue color lines) are shown.

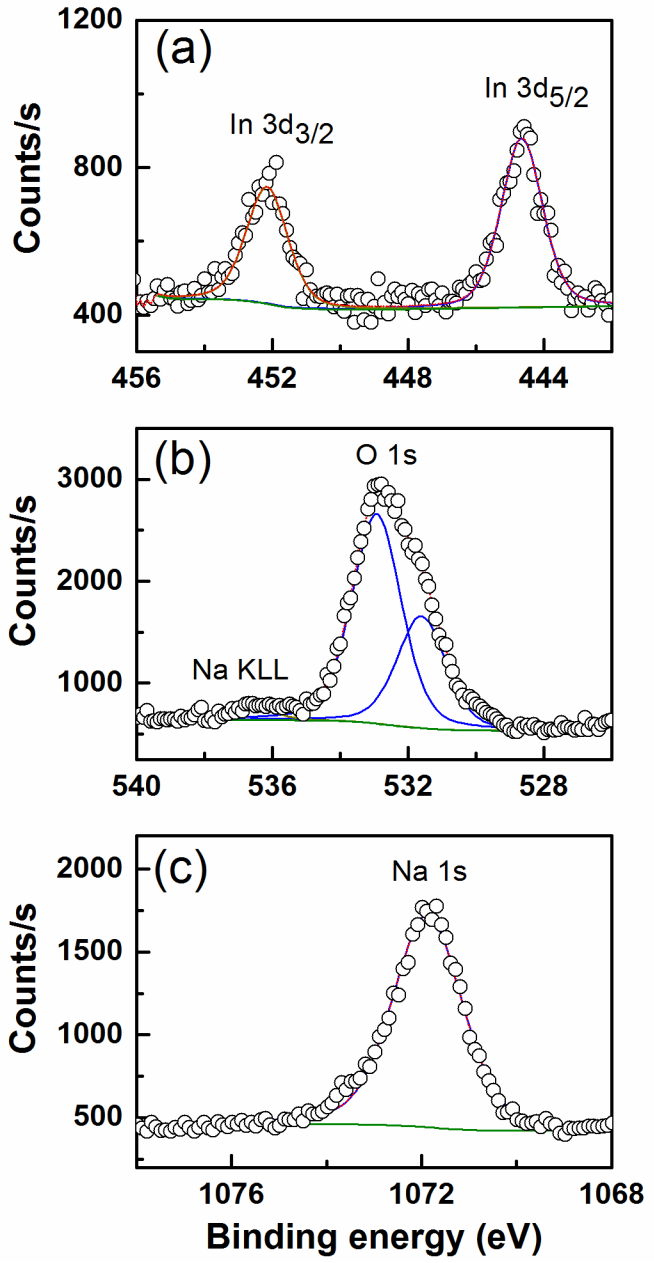

Figure 5-11 In 3d (a), O 1s (b), and Na 1s (b) XP spectra of the as-prepared indium oxide nanoparticulate films. Measured (black color circles) and fitted data (red color lines), deconvolution of O 1s (indium oxide as well as substrate, blue color lines) and background (green color line) are marked in the graphs.

5.3.4. Monochromatic UV-laser curing of indium oxide nanoparticles

Monochromatic UV-laser curing has also been performed for printed indium oxide nanoparticulate films. These films have also been characterized by SEM as well as XPS to determine bulk and surface morphologies, respectively. SEM images (**Figure 5-12**) show that the bulk morphology is unchanged before and after monochromatic UV-laser curing. In contrast, XPS studies (**Figure 5-11**) show that the characteristics of PAANa are completely different before and after monochromatic UV-laser curing. One of the carbon peaks that belong to C-O has almost disappeared from the spectra of laser cured sample. Intensities of other two C 1s peaks are also lower compared to as prepared as well as UV-visible light cured ones. It indicates that the decomposition of capping agent is much better than UV-visible light curing, which resulted in better electrical performance.

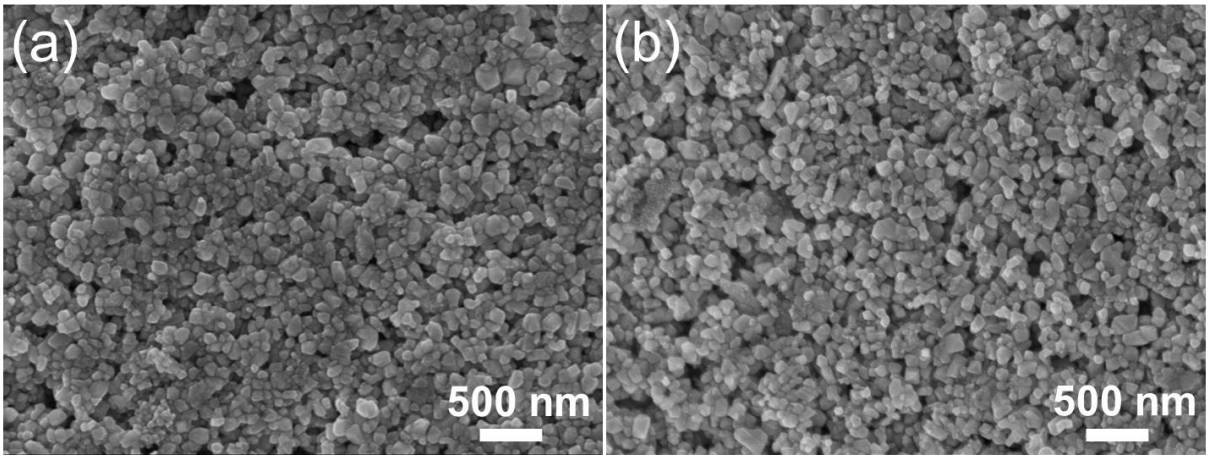

Figure 5-12 SEM images of indium oxide nanoparticulate films (a) before and (b) after monochromatic UV-laser curing (with a laser power of 6 mW).

5.4. Electrical characterization of UV-visible light and monochromatic UV-laser cured indium oxide precursor as well as nanoparticulate transistors

This section describes the electrical characterization of precursor and nanoparticulate based FETs treated by UV-visible light and UV-laser curing. Electrical characterization has been carried out at ambient conditions.

5.4.1. UV-visible light cured indium oxide precursor based transistors

Transfer and *I-V* characteristics of the devices cured for 60 and 90 s are shown in **Figure 5-13**. Both the FETs show low hysteresis, sharp subthreshold slopes (85 and 85 mV/decade), which is close to the theoretical limit (60 mV/decade), drain current ON/OFF ratios of 1.95×10^6, 4.4×10^7 and also positive threshold voltages (V_T of 0.4 and 0.0 V, respectively), i.e. enhancement mode MOSFET characteristics. However, the maximum drain currents (or ON current) are quite different (1.94 and 272 µA), which lead to different field-effect

mobilities (μ_{FET}), i.e. 2.4 and 50 $cm^2V^{-1}s^{-1}$. This is due to the difference in crystallinity, which is shown in the XRD patterns. The photonic curing process, in this sense is analogous to conventional annealing of indium oxide films at different temperatures where the films annealed at high annealing temperatures show better mobility due to improved crystallinity. The field-effect mobility of the devices has been calculated using the equation 2.1. All parameters are known for calculating the field-effect mobility except capacitance, which is once again considered to be the double layer capacitance of semiconductor (indium oxide) with respect to electrolyte. In fact, it can be derived based on the charging current of the device where parasitic capacitance is avoided by careful printing and the obtained value is 4.9 $\mu F/cm^2$ [135]. For all field-effect mobility calculations, this capacitance value has been used.

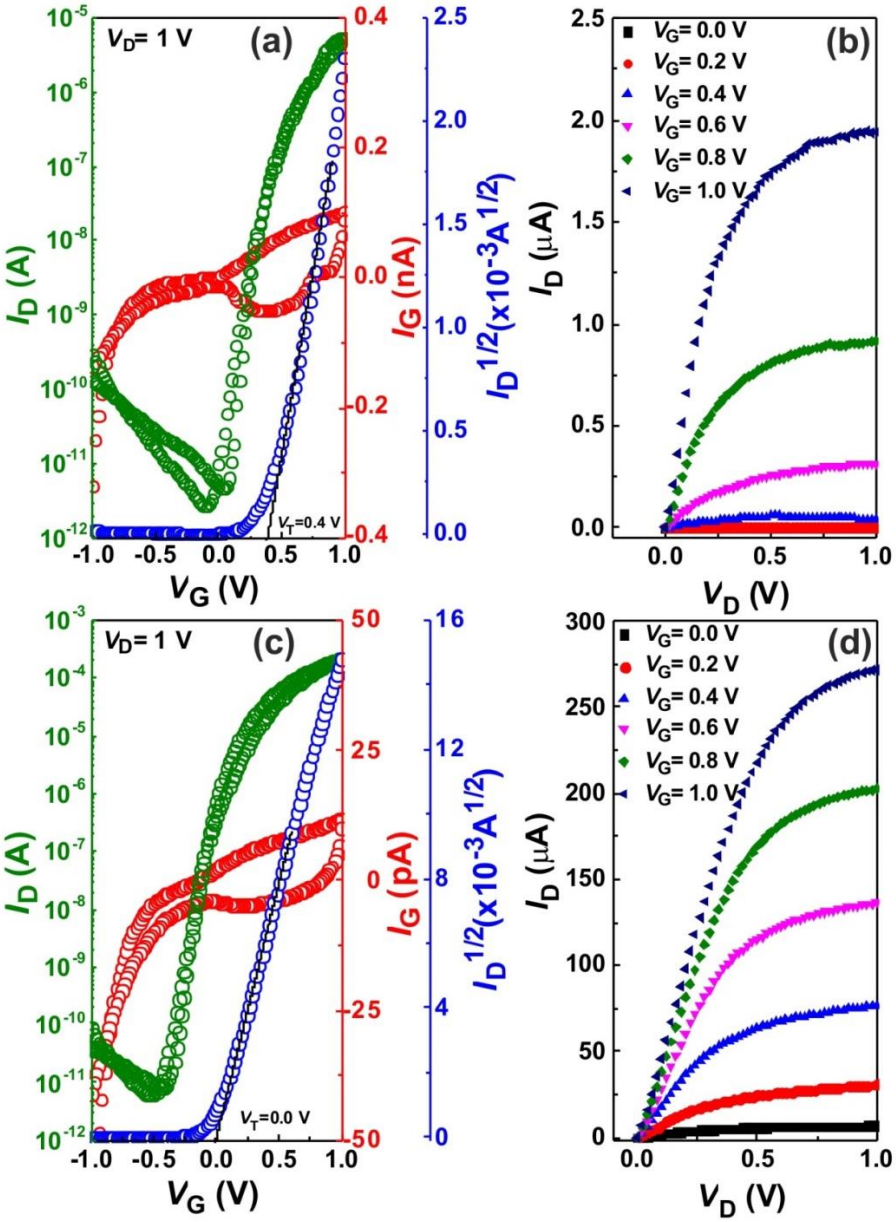

Figure 5-13 Transistor characteristics of UV-visible cured indium oxide precursor films for (a & b) 60 s and (c & d) 90 s pulses.

5.4.2. Monochromatic UV-laser cured indium oxide precursor based transistors

Electrical characterization has been performed for monochromatic UV-laser cured precursor based FETs. Transfer and *I-V* curves (**Figure 5-14**) show that the devices are in depletion mode with negative threshold voltage values (V_T = -0.3) with very low hysteresis. In addition, a subthreshold slope of 110 mV/decade and ON/OFF ratio of 1.2×10^6 are observed. However, the field-effect mobility (15 $cm^2V^{-1}s^{-1}$) is lower than UV-visible light cured FETs. The optimization of monochromatic UV-laser parameters such as monochromatic UV-laser power, the laser focus, and scan speed can improve it further.

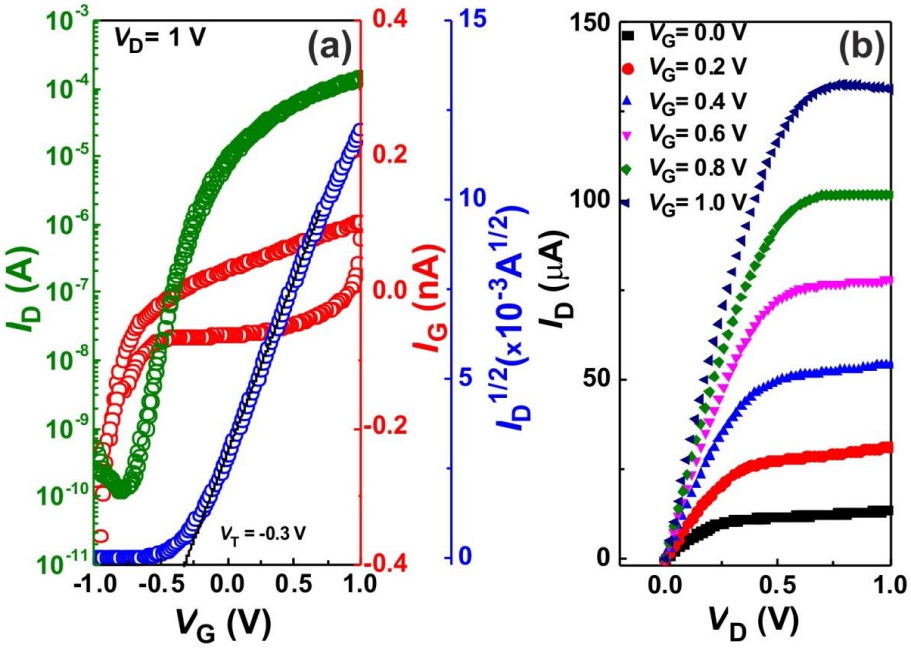

Figure 5-14 (a) Transfer and (b) *I-V* curves of monochromatic UV-laser cured (with a laser power of 53.5 mW) indium oxide precursor films.

Although the field effect mobility is lower than the UV-visible light cured FETs, monochromatic UV-laser curing has additional benefits, such as the laser is exposed only to the channel (due to small spot size of 10 μm), which reduces the damage of the substrate. Furthermore, variable scan speeds provide process flexibility for high throughput and also effect of irradiation to the environment is lower than the high energy UV-visible light pulses.

5.4.3. UV-visible light and monochromatic UV-laser cured indium oxide nanoparticulate based transistors

Electrical characterization has been carried out for the UV-visible light cured indium oxide nanoparticulate based FET devices. Transfer and *I-V* curves are shown in **Figure 5-15a&b**. The transfer curves show that the devices are in accumulation mode (V_T = 0.15 V) with an ON/OFF ratio of 2.2×10^6. The calculated subthreshold

slope is 110 mV/decade. The field-effect mobility is 8 $cm^2V^{-1}s^{-1}$, which is 8 times higher than that of the uncured films. In fact, the achieved mobility value is significantly higher for complete room temperature processed oxide FETs printed on flexible PEN substrates. This is because of the partial removal of the capping agent and the better electronic transport between the indium oxide nanoparticles due to UV-visible light curing process. On the other hand, *I-V* curves are linear in the initial stages and saturated thereafter. These curves also follow ideal quadratic behavior with a change in gate voltage. Moreover, these films have not shown any Schottky barrier: in this sense they are even superior to the chemically cured FETs, where extra ions (sodium chloride) are involved for the removal of capping agent.

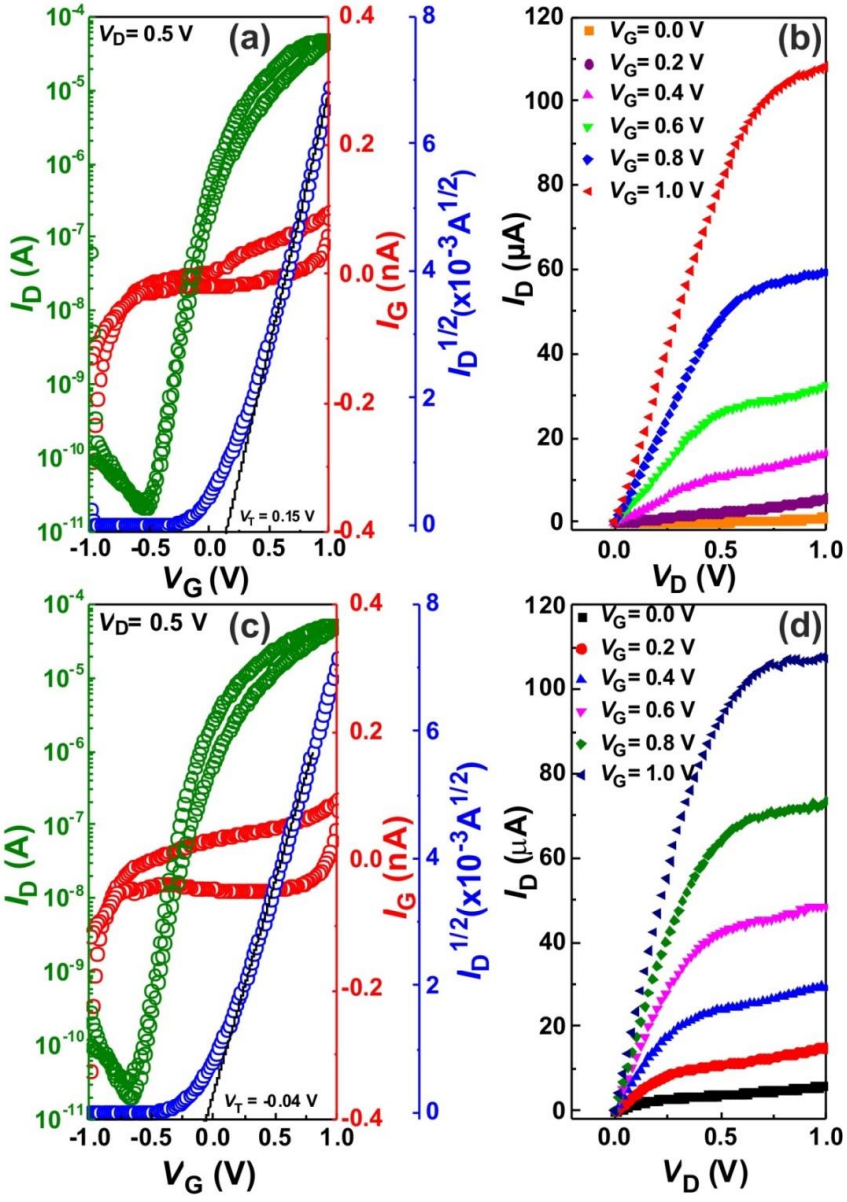

Figure 5-15 Transistor characteristics of (a & b) UV-visible light cured (pulses for 10 s) and (c & d) monochromatic UV-laser cured (with a laser power of 6 mW) indium oxide nanoparticulate films.

Electrical characterization has also been carried out for UV-laser cured nanoparticulate films. Transistor characteristics (**Figure 5-15c&d**) show that the devices are in depletion mode with a negative threshold voltage (V_T = -0.04 V). The ON/OFF ratio and field-effect mobility values are 1.2 $\times 10^6$, 12 $cm^2V^{-1}s^{-1}$, respectively. The achieved mobility value is 1.5 times higher than UV-visible light cured transistors and close to chemically cured FETs. The reason for a high mobility value is the removal of the capping agent which in fact is even better than for UV-visible light cured films, resulting in a better electronic transport.

In summary, the indium oxides FETs have been prepared by inkjet printing and cured by photonic curing techniques, such as broad wavelength UV-visible light and monochromatic UV-laser curing. Precursor and nanoparticles based FETs have been printed on inexpensive glass and flexible PEN substrates, respectively. For precursors, high energies (both UV-visible light and monochromatic UV-laser) were used to obtain crystalline indium oxide from indium nitrate precursors. UV-visible light cured precursor based FETs have shown high performance (50 $cm^2V^{-1}s^{-1}$) when compared to monochromatic UV-laser cured FETs (15 $cm^2V^{-1}s^{-1}$). On the other hand, nanoparticulate FETs have been prepared by printing dispersed indium oxide NPs which have PAANa as the capping agent. For NPs FETs, very low energies are used to cure the nanoparticles. Both UV-visible light and monochromatic UV-laser decomposed the capping agent and ensured better electronic transport which resulted in good performance of the FETs. The achieved mobility values for UV-visible light and monochromatic UV-lasers are 8 and 12 $cm^2V^{-1}s^{-1}$ respectively. These results indicate that photonic curing (either UV-visible light or monochromatic UV-laser) is useful to realize high performance solution processed oxide FETs which can be prepared on inexpensive glass as well as PEN substrates. These results also pave the way to realize portable and thin film battery compatible printed electronics.

6. Conclusions and Outlook

6.1. Conclusions

In the present thesis, the fabrication and the characterization of printed oxide FETs and logics (CMOS inverters and amplifiers) have been demonstrated. Both n- and p-type oxide semiconductors (In_2O_3, CuO) have been chosen as channel materials. An easy-to-print composite solid polymer electrolyte has been used as the gate insulator. First, high performance FETs and logics have been prepared by precursor route, involving an annealing routine at high (400 °C) temperatures. In the next step, to reduce process temperatures, novel chemical curing method was explored for oxide nanoparticulate FETs. In order to further enhance the performance of the low temperature-processed FETs, novel techniques such as UV-visible light and monochromatic UV-laser curing have also been investigated, both for precursor-based as well as nanoparticulate channel based FETs. The major outcomes of this thesis are:

1. In_2O_3 channel FETs have been prepared from an inkjet printed indium chloride precursor and subsequently annealed at different temperatures (300-500 °C) with varying heating rates. The one, which is annealed at 400 °C, has shown the highest value of μ_{FET} of 126 $cm^2V^{-1}s^{-1}$. The reasons for such a high mobility are formation of phase pure indium oxide with large crystallite sizes and an extremely conformal semiconductor-dielectric interface between the In_2O_3 films and the printed electrolyte layer. The effect of heating rate on the performance of oxide transistors has also been studied. The slow heated precursors (1 °C/min) have shown better performance when compared to the ones which are directly inserted at particular temperature.

2. In order to realize complementary circuits, it is also necessary to fabricate FETs with hole conducting *p*-type semiconductors. CuO is one of the stable p-type semiconductors that can be easily prepared with solution processing. Therefore, CuO has been chosen to fabricate p-channel FETs. With the identical fabrication routine, a mobility of 0.22 $cm^2V^{-1}s^{-1}$ has been achieved for p-type CuO transistors. Although the mobility of CuO is rather low when compared to In_2O_3, it is possible to combine them to construct complementary logics. Therefore, CMOS inverters and amplifiers were prepared using these two oxide semiconductors. The CMOS inverter has shown a signal gain of 21 at 1.5 V with low static power consumption. Common source amplifier showed a gain of 5 at very low drive voltages (0.5 V) with low power consumption even when it is in the dynamic mode.

3. A novel chemical curing method has been investigated, which can simultaneously eliminate high process temperatures, and can also ensure dense nanoparticulate film formation resulting in superior electrical performance. In the chemical curing method, along with In_2O_3 nanoparticles, polyelectrolyte (poly acrylic acid of sodium salt, PAANa) as stabilizer and NaCl as the destabilizing agent are added to form the nanoink. During

the drying process of the printed nanoink, NaCl detaches the PAANa-surfactant from the surfaces of the nanoparticles, which on one hand helps to improve the interparticle contacts and on the other hand ensures densification of the printed nanoparticulate film. Consequently, significant improvement in the performance of the printed transistors has been noticed. In this case, room temperature printed and cured indium oxide nanoparticles as the transistor channel FETs demonstrate a field-effect mobility of 12.5 $cm^2V^{-1}s^{-1}$, which is by far the best performance achieved for printed oxide FETs processed at room temperature. Using the same method, a CMOS inverter (n-type In_2O_3 and p-type Cu_2O nanoparticles) has also been prepared which shows a signal gain of 18 with very low power consumption.

4. In addition, the effect of photonic curing on nanoparticulate films has also been studied. Photonic curing techniques can be used to realize low temperature electronics. A monochromatic UV-laser is used to convert the precursors into respective oxides on transparent glass substrates. The same method can also be used to remove stabilizers from nanoparticle surface and densify/sinter the nanoparticles together. Taking advantage of the fact that the energy is absorbed mostly by the nanoparticulate layer, this method of local heating allows the use of low-softening temperature polymer substrates such as polyethylene naphthalate. In both cases, device performance, e.g. device mobility has largely been improved compared to the non-treated films. Indium oxide nanoparticles as well as precursor based FETs have shown a mobility of 12 and 15 cm^2/Vs, respectively. Another technique, i.e. UV-visible light curing has been implemented, which has the potential to cure the films within a few seconds (due to very high energy pulses). This method, however, is a global heating technique, and the incident energy is homogeneously distributed for large areas. Therefore, on one hand, in this case, the substrate material receives significant amount of UV-radiation, however, on the other hand, a large area of substrate and a significant number of devices can be cured simultaneously. With UV-visible light pulses applied for 90 s for indium oxide precursor based FETs mobility values of 50 $cm^2V^{-1}s^{-1}$ have been achieved, whereas indium oxide nanoparticulate FETs have shown a mobility of 8 $cm^2V^{-1}s^{-1}$.

The results indicate the potential of oxide semiconductors for high performance printed FETs and logics. Along with oxides, the (choice of) electrolyte also played a crucial role in realizing such high field effect mobility devices. The demonstration of high performance devices by different methods such as chemical and photonic curing indicates that these are suitable for low power battery compatible and portable electronic applications.

6.2. Outlook

Oxide semiconductors (channel) and electrolyte (gate insulator) have been proven to be highly suitable materials for achieving high performance solution processed/printed FETs and CMOS logics. However, there is yet a long way to go before this technology is matured enough to be considered for applications. Therefore, it is rather not a difficult task to propose a long list of future studies that would be essential, interesting and important. Here only a few of those possible outlooks are enlisted.

1. A major portion of the present work involved the preparation of single FETs, however, to realize printed circuits, it is not sufficient to only consider high performance single FETs. There may be a long list of circuit level problems that are not possible to foresee at this stage. Consequently, one should now concentrate to realize at least simple logics, such as AND, OR, NAND, NOR etc. Moreover the high frequency performance should be tested with ring oscillators, D-flipflops etc. In achieving this, issues such as parasitic capacitance (one of the major concern for electrolyte gated FETs), leakage currents, bias stress stability, etc., need to be addressed.

2. More often than not, printed devices suffer from variability, i.e., variable performance in individual FETs. The reasons for such a different performance are mostly related to the printing process itself, such as, substrate surface, change in drop volume, clogging of nozzles, change in ink behavior, etc. In this aspect, a comprehensive study toward addressing this printing related variability issues would be highly welcome. In fact, this effort should precede those of building further complex circuit elements. In other words, without an improved control over reproducibility in device characteristics, it may not be sensible to try to increase complexity in printed logics.

3. Although, the chemical and photonic curing techniques have been explored in the present thesis, the achieved mobility values are still lower than the conventional heat-treated (annealed) devices. In this regard, a new method, i.e., combination of in-situ reduction (using inherent reducing agent in the precursor) and photonic curing (in order to enhance reaction kinetics) will be investigated to realize oxide semiconductor phases from respective precursors. There will be no annealing step involved in this method and the photonic treatment will also be for rather short duration. Consequently, it is likely that the process will enable preparation of oxide semiconductors on inexpensive substrates. This method will provide phase-pure semiconductor material with good film quality. As a result, improved electrical performance can be achieved.

Curriculum Vitae

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List of Publications

Published

1. SK Garlapati, N Mishra, S Dehm, R Hahn, R Kruk, H Hahn, S Dasgupta, "Electrolyte-gated, high mobility inorganic oxide transistors from printed metal halides", **ACS applied materials & interfaces** 2013, 5 (22), 11498-11502.

2. SK Garlapati, TT Baby, S Dehm, M Hammad, VSK Chakravadhanula, R Kruk, H Hahn, S Dasgupta, "Ink-Jet Printed CMOS Electronics from Oxide Semiconductors", **Small** 2015, 11 (29), 3591–3596.
3. TT Baby, SK Garlapati, S Dehm, M Häming, R Kruk, H Hahn, S Dasgupta, "A General Route toward Complete Room Temperature Processing of Printed and High Performance Oxide Electronics", **ACS Nano** 2015, 9 (3), 3075-3083.
4. J Liu, W Zhou, J Liu, Y Fujimori, T Higashino, H Imahori, X Jiang, J Zhao, T Sakurai, Y Hattori, W Matsuda, S Seki, SK Garlapati, S Dasgupta, E Redel, L Sun, C Wöll, "A new class of epitaxial porphyrin metal–organic framework thin films with extremely high photocarrier generation efficiency: promising materials for all-solid-state solar cells", **Journal of Materials Chemistry A** 2016, 4 (33), 12739-12747.
5. GC Marques, SK Garlapati, D Chatterjee, S Dehm, S Dasgupta, J Aghassi and MB Tahoori, "Electrolyte-gated FETs based on oxide semiconductors: fabrication and modeling", **IEEE Transactions on Electron Devices** 2017, 64, 279-285.
6. M Häming, TT Baby, SK Garlapati, B Krause, H Hahn, S Dasgupta, L Weinhardt, C Heske, "The effect of NaCl on room-temperature-processed indium oxide nanoparticle thin films for printed electronics", **Applied Surface Science** 2017, 396, 912-919.
7. AS Parvathy, A Molinari, A Benes, C Loho, VSK Chakravadhanula, SK Garlapati, R Kruk, O Clemens, "Conductivity study of thin epitaxial films of barium ferrite and their hydrated forms $BaFeO_{2.5-x+\delta}(OH)_{2x}$", accepted by **Journal of Physics D: Applied Physics** (2017).

Submitted

8. SK Garlapati, JS Gebauer, S Dehm, M Winterer, H Hahn, S Dasgupta, "Room temperature processing of printed oxide FETs using ultra-violet photonic curing", submitted to **Advanced Electronic Materials** (2016).

To be submitted

9. SK Garlapati, S Dehm, H Hahn, S Dasgupta, "Solution processed composite dielectric for printed oxide FETs", to be submitted.
10. BK Sharma, A Stoesser, SK Garlapati, S Dehm, V. S. K Chakravadhanula, R Kruk, H Hahn, S Dasgupta, "All printed amorphous oxide In-Ga-ZnO based field effect transistor and logic circuits with electrolyte gating", to be submitted.
11. N Mishra, SM Yi, SK Garlapati, S Dasgupta, H Hahn, O Kraft and P Gruber, "Mechanical study of electrolyte-gated, ink-jet printed high mobility indium oxide transistors on flexible substrate", to be submitted.

References

[1] S. Okamura, *History of electron tubes*: IOS Press, 1994.

[2] E. Fortunato, P. Barquinha, and R. Martins, "Oxide semiconductor thin-film transistors: a review of recent advances", *Advanced Materials,* vol. 24, pp. 2945-86, 2012.

[3] S. Jeong and J. Moon, "Low-temperature, solution-processed metal oxide thin film transistors", *Journal of Materials Chemistry,* vol. 22, pp. 1243-1250, 2012.

[4] J. J. Schneider, R. C. Hoffmann, J. Engstler, O. Soffke, W. Jaegermann, A. Issanin, and A. Klyszcz, "A Printed and Flexible Field-Effect Transistor Device with Nanoscale Zinc Oxide as Active Semiconductor Material", *Advanced Materials,* vol. 20, pp. 3383-3387, 2008.

[5] B. S. Ong, C. Li, Y. Li, Y. Wu, and R. Loutfy, "Stable, solution-processed, high-mobility ZnO thin-film transistors", *Journal of the American Chemical Society,* vol. 129, pp. 2750-2751, 2007.

[6] R. Theissmann, S. Bubel, M. Sanlialp, C. Busch, G. Schierning, and R. Schmechel, "High performance low temperature solution-processed zinc oxide thin film transistor", *Thin Solid Films,* vol. 519, pp. 5623-5628, 2011.

[7] H. Faber, M. Burkhardt, A. Jedaa, D. Kälblein, H. Klauk, and M. Halik, "Low-Temperature Solution-Processed Memory Transistors Based on Zinc Oxide Nanoparticles", *Advanced Materials,* vol. 21, pp. 3099-3104, 2009.

[8] M. Singh, H. M. Haverinen, P. Dhagat, and G. E. Jabbour, "Inkjet printing-process and its applications", *Advanced Materials,* vol. 22, pp. 673-85, 2010.

[9] R. Parashkov, E. Becker, T. Riedl, H.-H. Johannes, and W. Kowalsky, "Large area electronics using printing methods", *Proceedings of the IEEE,* vol. 93, pp. 1321-1329, 2005.

[10] M. L. Chabinyc, W. S. Wong, A. C. Arias, S. Ready, R. A. Lujan, J. H. Daniel, B. Krusor, R. B. Apte, A. Salleo, and R. A. Street, "Printing methods and materials for large-area electronic devices", *Proceedings of the IEEE,* vol. 93, pp. 1491-1499, 2005.

[11] M. J. Panzer and C. D. Frisbie, "Exploiting Ionic Coupling in Electronic Devices: Electrolyte-Gated Organic Field-Effect Transistors", *Advanced Materials,* vol. 20, pp. 3177-3180, 2008.

[12] D. J. Carrad, A. M. Burke, R. W. Lyttleton, H. J. Joyce, H. H. Tan, C. Jagadish, K. Storm, H. Linke, L. Samuelson, and A. P. Micolich, "Electron-beam patterning of polymer electrolyte films to make multiple nanoscale gates for nanowire transistors", *Nano Letters,* vol. 14, pp. 94-100, 2014.

[13] L. Kergoat, L. Herlogsson, D. Braga, B. Piro, M. C. Pham, X. Crispin, M. Berggren, and G. Horowitz, "A water-gate organic field-effect transistor", *Advanced Materials,* vol. 22, pp. 2565-9, 2010.

[14] S. Sze and K. K. Ng, *Physics of semiconductor devices,* 3rd Ed., John Wiley & Sons, 2007.

[15] J.-P. Colinge and C. A. Colinge, *Physics of semiconductor devices,* Springer Science & Business Media, 2005.

[16] Y. Sakai, T. Masuhara, O. Minato, and N. Hashimoto, "High packing density, high speed CMOS (Hi-CMOS) device technology", *Japanese Journal of Applied Physics*, vol. 18, p. 73, 1979.

[17] N. Weste, D. Harris, *CMOS VLSI Design: A Circuits And Systems Perspective*, Addison-Wesley, 2011.

[18] B. G. Streetman, *Solid state electronic devices*, Prentice Hall, Inc., New Jersey, 1995.

[19] Y. Sun and J. A. Rogers, "Inorganic Semiconductors for Flexible Electronics", *Advanced Materials*, vol. 19, pp. 1897-1916, 2007.

[20] S. R. Thomas, P. Pattanasattayavong, and T. D. Anthopoulos, "Solution-processable metal oxide semiconductors for thin-film transistor applications", *Chemical Society Review*, vol. 42, pp. 6910-23, 2013.

[21] M. Marezio, "Refinement of the crystal structure of In_2O_3 at two wavelengths", *Acta Crystallographica*, vol. 20, pp. 723-728, 1966.

[22] S. H. Brewer and S. Franzen, "Calculation of the electronic and optical properties of indium tin oxide by density functional theory", *Chemical Physics*, vol. 300, pp. 285-293, 2004.

[23] P. D. King, T. D. Veal, D. J. Payne, A. Bourlange, R. G. Egdell, and C. F. McConville, "Surface electron accumulation and the charge neutrality level in In_2O_3", *Physical Review Letters*, vol. 101, p. 116808, 2008.

[24] R. L. Weiher, "Electrical Properties of Single Crystals of Indium Oxide", *Journal of Applied Physics*, vol. 33, p. 2834, 1962.

[25] J. H. Noh, S. Y. Ryu, S. J. Jo, C. S. Kim, S.-W. Sohn, P. D. Rack, D.-J. Kim, and H. K. Baik, "Indium oxide thin-film transistors fabricated by RF sputtering at room temperature", *IEEE Electron Device Letters*, vol. 31, pp. 567-569, 2010.

[26] A. Walsh, J. L. Da Silva, S. H. Wei, C. Korber, A. Klein, L. F. Piper, A. DeMasi, K. E. Smith, G. Panaccione, P. Torelli, D. J. Payne, A. Bourlange, and R. G. Egdell, "Nature of the band gap of In_2O_3 revealed by first-principles calculations and X-ray spectroscopy", *Physical Review Letters*, vol. 100, p. 167402, 2008.

[27] S. Cho, "Effects of rapid thermal annealing on the properties of In_2O_3 thin films grown on glass substrate by rf reactive magnetron sputtering", *Microelectronic Engineering*, vol. 89, pp. 84-88, 2012.

[28] N. Taga, Y. Shigesato, and M. Kamei, "Electrical properties and surface morphology of heteroepitaxial-grown tin-doped indium oxide thin films deposited by molecular-beam epitaxy", *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 18, p. 1663, 2000.

[29] M. H. Lee, C. C. Shih, J. S. Chen, W. M. Huang, F. Y. Gan, Y. C. Shih, C. X. Qiu, and I. Shih, "Excellent Performance of Indium-Oxide-Based Thin-Film Transistors by DC Sputtering", in *SID Symposium Digest of Technical Papers*, vol. 40, pp. 191-193, 2009.

[30] S. Suh and D. M. Hoffman, "General synthesis of homoleptic indium alkoxide complexes and the chemical vapor deposition of indium oxide films", *Journal of American Chemical Society*, vol. 122, pp. 9396-9404, 2000.

[31] M. Girtan and G. Folcher, "Structural and optical properties of indium oxide thin films prepared by an ultrasonic spray CVD process", *Surface and Coatings Technology*, vol. 172, pp. 242-250, 2003.

[32] J. Kane, H. Schweizer, and W. Kern, "Chemical vapor deposition of transparent electrically conducting layers of indium oxide doped with tin", *Thin Solid Films*, vol. 29, pp. 155-163, 1975.

[33] R. Bel Hadj Tahar, T. Ban, Y. Ohya, and Y. Takahashi, "Optical, structural, and electrical properties of indium oxide thin films prepared by the sol-gel method", *Journal of Applied Physics*, vol. 82, p. 865, 1997.

[34] R. Bel Hadj Tahar, T. Ban, Y. Ohya, and Y. Takahashi, "Electronic transport in tin-doped indium oxide thin films prepared by sol-gel technique", *Journal of Applied Physics*, vol. 83, p. 2139, 1998.

[35] W.-Y. Chung, G. Sakai, K. Shimanoe, N. Miura, D.-D. Lee, and N. Yamazoe, "Preparation of indium oxide thin film by spin-coating method and its gas-sensing properties", *Sensors and Actuators B: Chemical*, vol. 46, pp. 139-145, 1998.

[36] P.-C. Chen, G. Shen, H. Chen, Y.-g. Ha, C. Wu, S. Sukcharoenchoke, Y. Fu, J. Liu, A. Facchetti, and T. J. Marks, "High-performance single-crystalline arsenic-doped indium oxide nanowires for transparent thin-film transistors and active matrix organic light-emitting diode displays", *ACS Nano*, vol. 3, pp. 3383-3390, 2009.

[37] J. H. Kim, T.-Y. Seong, S.-I. Na, K.-B. Chung, H.-M. Lee, and H.-K. Kim, "Highly transparent Nb-doped indium oxide electrodes for organic solar cells", *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 32, p. 021202, 2014.

[38] T. Jäger, Y. E. Romanyuk, S. Nishiwaki, B. Bissig, F. Pianezzi, P. Fuchs, C. Gretener, M. Döbeli, and A. N. Tiwari, "Hydrogenated indium oxide window layers for high-efficiency Cu(In,Ga)Se_2 solar cells", *Journal of Applied Physics*, vol. 117, p. 205301, 2015.

[39] E. L. Runnerstrom, A. Llordes, S. D. Lounis, and D. J. Milliron, "Nanostructured electrochromic smart windows: traditional materials and NIR-selective plasmonic nanocrystals", *Chemical Communications (Cambridge)*, vol. 50, pp. 10555-72, 2014.

[40] G. Korotcenkov, V. Brinzari, A. Cornet, and J. Morante, "Experimental and theoretical studies of indium oxide gas sensors fabricated by spray pyrolysis", *Sensors and Actuators B: Chemical*, vol. 106, pp. 563-571, 2005.

[41] M. Suchea, N. Katsarakis, S. Christoulakis, S. Nikolopoulou, and G. Kiriakidis, "Low temperature indium oxide gas sensors", *Sensors and Actuators B: Chemical*, vol. 118, pp. 135-141, 2006.

[42] D. Wu, Q. Zhang, and M. Tao, "LSDA+ U study of cupric oxide: electronic structure and native point defects", *Physical Review B*, vol. 73, p. 235206, 2006.

[43] S. Åsbrink and L.-J. Norrby, "A refinement of the crystal structure of copper (II) oxide with a discussion of some exceptional esd's", *Acta Crystallographica Section B: Structural Crystallography and Crystal Chemistry*, vol. 26, pp. 8-15, 1970.

[44] A. Samokhvalov, N. Viglin, B. Gizhevskij, N. Loshkareva, V. Osipov, N. Solin, and Y. P. Sukhorukov, "Low-mobility charge carriers in CuO", *Zhurnal Eksperimentalnoi i Teoreticheskoi Fiziki*, vol. 103, pp. 951-961, 1993.

[45] S. Masudy-Panah, G. K. Dalapati, K. Radhakrishnan, A. Kumar, H. R. Tan, E. Naveen Kumar, C. Vijila, C. C. Tan, and D. Chi, "p-CuO/n-Si heterojunction solar cells with high open circuit voltage and photocurrent through interfacial engineering", *Progress in Photovoltaics: Research and Applications*, vol. 23, pp. 637-645, 2015.

[46] Y.-S. Kim, I.-S. Hwang, S.-J. Kim, C.-Y. Lee, and J.-H. Lee, "CuO nanowire gas sensors for air quality control in automotive cabin", *Sensors and Actuators B: Chemical*, vol. 135, pp. 298-303, 2008.

[47] E. Fortin and F. Weichman, "Hall effect and electrical conductivity of Cu_2O monocrystals", *Canadian Journal of Physics*, vol. 44, pp. 1551-1561, 1966.

[48] E. Ruiz, S. Alvarez, P. Alemany, and R. A. Evarestov, "Electronic structure and properties of Cu_2O", *Physical Review B*, vol. 56, p. 7189, 1997.

[49] M. Yin, C. K. Wu, Y. Lou, C. Burda, J. T. Koberstein, Y. Zhu, and S. O'Brien, "Copper oxide nanocrystals", *Journal of the American Chemical Society*, 127, pp. 9506-11, 2005.

[50] S. Poulston, P. Parlett, P. Stone, and M. Bowker, "Surface oxidation and reduction of CuO and Cu_2O studied using XPS and XAES", *Surface and Interface Analysis*, vol. 24, pp. 811-820, 1996.

[51] H. Du, X. Lin, Z. Xu, and D. Chu, "Electric double-layer transistors: a review of recent progress", *Journal of Materials Science*, vol. 50, pp. 5641-5673, 2015.

[52] S. Srinivasan, "Electrode/electrolyte interfaces: Structure and kinetics of charge transfer", in *Fuel Cells*, ed: Springer, pp. 27-92, 2006.

[53] S. H. Kim, K. Hong, W. Xie, K. H. Lee, S. Zhang, T. P. Lodge, and C. D. Frisbie, "Electrolyte-gated transistors for organic and printed electronics", *Advanced Materials*, vol. 25, pp. 1822-46, 2013.

[54] L. Santos, D. Nunes, T. Calmeiro, R. Branquinho, D. Salgueiro, P. Barquinha, L. Pereira, R. Martins, and E. Fortunato, "Solvothermal synthesis of gallium-indium-zinc-oxide nanoparticles for electrolyte-gated transistors", *ACS Applied Materials & Interfaces*, vol. 7, pp. 638-46, 2015.

[55] J. Ko, S. J. Lee, K. Kim, E. Lee, K.-H. Lim, J.-M. Myoung, J. Yoo, and Y. S. Kim, "A robust ionic liquid–polymer gate insulator for high-performance flexible thin film transistors", *Journal of Materials Chemistry C*, vol. 3, pp. 4239-4243, 2015.

[56] K. Hong, S. H. Kim, K. H. Lee, and C. D. Frisbie, "Printed, sub-2V ZnO electrolyte gated transistors and inverters on plastic", *Advanced Materials*, vol. 25, pp. 3413-8, 2013.

[57] S. Thiemann, S. Sachnov, S. Porscha, P. Wasserscheid, and J. Zaumseil, "Ionic Liquids for Electrolyte-Gating of ZnO Field-Effect Transistors", *The Journal of Physical Chemistry C*, vol. 116, pp. 13536-13544, 2012.

[58] S. Dasgupta, R. Kruk, N. Mechau, and H. Hahn, "Inkjet printed, high mobility inorganic-oxide field effect transistors processed at room temperature", *ACS Nano*, vol. 5, pp. 9628-38, 2011.

[59] J. Kofler, K. Schmoltner, A. Klug, and E. J. W. List-Kratochvil, "Hydrogen ion-selective electrolyte-gated organic field-effect transistor for pH sensing", *Applied Physics Letters*, vol. 104, p. 193305, 2014.

[60] J. Sayago, F. Soavi, Y. Sivalingam, F. Cicoira, and C. Santato, "Low voltage electrolyte-gated organic transistors making use of high surface area activated carbon gate electrodes", *Journal of Materials Chemistry C*, vol. 2, p. 5690, 2014.

[61] D. Wang, V. Noël, and B. Piro, "Electrolytic Gated Organic Field-Effect Transistors for Application in Biosensors-A Review", *Electronics*, vol. 5, p. 9, 2016.

[62] C. Mackin and T. Palacios, "Large-scale sensor systems based on graphene electrolyte-gated field-effect transistors", *Analyst*, vol. 141, pp. 2704-11, 2016.

[63] M.-W. Lin, L. Liu, Q. Lan, X. Tan, K. S. Dhindsa, P. Zeng, V. M. Naik, M. M.-C. Cheng, and Z. Zhou, "Mobility enhancement and highly efficient gating of monolayer MoS_2 transistors with polymer electrolyte", *Journal of Physics D: Applied Physics*, vol. 45, p. 345102, 2012.

[64] E. Lhuillier, S. Pedetti, S. Ithurria, H. Heuclin, B. Nadal, A. Robin, G. Patriarche, N. Lequeux, and B. Dubertret, "Electrolyte-Gated Field Effect Transistor to Probe the Surface Defects and Morphology in Films of Thick CdSe Colloidal Nanoplatelets", *ACS Nano*, vol. 8, pp. 3813-3820, 2014/04/22 2014.

[65] D. B. Mitzi, "Solution-processed inorganic semiconductors", *Journal of Materials Chemistry*, vol. 14, p. 2355, 2004.

[66] Y. J. Kwack and W. S. Choi, "Electrohydrodynamic Jet Printed Indium-Zinc-Oxide Thin-Film Transistors", *Journal of Display Technology*, vol. 12, pp. 3-7, 2016.

[67] D. Wan, X. Liu, L. Xu, C. Liu, X. Xiao, S. Guo, and L. Liao, "The Study for Solution-Processed Alkali Metal-Doped Indium-Zinc Oxide Thin-Film Transistors," *IEEE Electron Device Letters*, vol. 37, pp. 50-52, 2016.

[68] V. Pecunia, K. Banger, and H. Sirringhaus, "High-Performance Solution-Processed Amorphous-Oxide-Semiconductor TFTs with Organic Polymeric Gate Dielectrics", *Advanced Electronic Materials*, vol. 1, pp. n/a-n/a, 2015.

[69] W. J. Lee, W. T. Park, S. Park, S. Sung, Y. Y. Noh, and M. H. Yoon, "Large-Scale Precise Printing of Ultrathin Sol-Gel Oxide Dielectrics for Directly Patterned Solution-Processed Metal Oxide Transistor Arrays", *Advanced Materials*, vol. 27, pp. 5043-8, 2015.

[70] X. Yu, J. Smith, N. Zhou, L. Zeng, P. Guo, Y. Xia, A. Alvarez, S. Aghion, H. Lin, J. Yu, R. P. Chang, M. J. Bedzyk, R. Ferragut, T. J. Marks, and A. Facchetti, "Spray-combustion synthesis: efficient solution route to high-performance oxide transistors", *Proceedings of the National Academy of Sciences, USA*, vol. 112, pp. 3217-22, 2015.

[71] P. K. Nayak, M. N. Hedhili, D. Cha, and H. N. Alshareef, "High performance In_2O_3 thin film transistors using chemically derived aluminum oxide dielectric", *Applied Physics Letters*, vol. 103, p. 033518, 2013.

[72] S. Y. Han, G. S. Herman, and C. H. Chang, "Low-temperature, high-performance, solution-processed indium oxide thin-film transistors", *Journal of the American Chemical Society,* vol. 133, pp. 5166-9, 2011.

[73] M. G. Kim, M. G. Kanatzidis, A. Facchetti, and T. J. Marks, "Low-temperature fabrication of high-performance metal oxide thin-film electronics via combustion processing", *Nature Materials,* vol. 10, pp. 382-8, 2011.

[74] H. S. Kim, P. D. Byrne, A. Facchetti, and T. J. Marks, "High performance solution-processed indium oxide thin-film transistors", *Journal of the American Chemical Society,* vol. 130, pp. 12580-1, 2008.

[75] J. Yu, G. Liu, A. Liu, Y. Meng, B. Shin, and F. Shan, "Solution-processed p-type copper oxide thin-film transistors fabricated by using a one-step vacuum annealing technique", *Journal of Materials Chemistry C,* vol. 3, pp. 9509-9513, 2015.

[76] P. Pattanasattayavong, S. Thomas, G. Adamopoulos, M. A. McLachlan, and T. D. Anthopoulos, "p-channel thin-film transistors based on spray-coated Cu_2O films", *Applied Physics Letters,* vol. 102, p. 163505, 2013.

[77] S. Y. Kim, C. H. Ahn, J. H. Lee, Y. H. Kwon, S. Hwang, J. Y. Lee, and H. K. Cho, "p-Channel oxide thin film transistors using solution-processed copper oxide", *ACS Applied Materials & Interfaces,* vol. 5, pp. 2417-21, 2013.

[78] Y. Neuvo and S. Ylönen, *Bit Bang-Rays to the Future*, Helsinki University Print, Helsinki, vol. 63, 2009.

[79] E. Tekin, P. J. Smith, and U. S. Schubert, "Inkjet printing as a deposition and patterning tool for polymers and inorganic particles", *Soft Matter,* vol. 4, p. 703, 2008.

[80] P. J. Yunker, T. Still, M. A. Lohr, and A. G. Yodh, "Suppression of the coffee-ring effect by shape-dependent capillary interactions", *Nature,* vol. 476, pp. 308-11, 2011.

[81] J. Cesarano, I. A. Aksay, and A. Bleier, "Stability of Aqueous α-Al_2O_3 Suspensions with Poly (methacrylic acid) Polyelectrolyte", *Journal of the American Chemical Society,* vol. 71, pp. 250-255, 1988.

[82] C. H. Choi, L. Y. Lin, C. C. Cheng, and C. h. Chang, "Printed Oxide Thin Film Transistors: A Mini Review", *ECS Journal of Solid State Science and Technology,* vol. 4, pp. P3044-P3051, 2015.

[83] K. K. Banger, Y. Yamashita, K. Mori, R. L. Peterson, T. Leedham, J. Rickard, and H. Sirringhaus, "Low-temperature, high-performance solution-processed metal oxide thin-film transistors formed by a 'sol-gel on chip' process," *Nature Materials,* vol. 10, pp. 45-50, 2011.

[84] Y. H. Kim, J. S. Heo, T. H. Kim, S. Park, M. H. Yoon, J. Kim, M. S. Oh, G. R. Yi, Y. Y. Noh, and S. K. Park, "Flexible metal-oxide devices made by room-temperature photochemical activation of sol-gel films", *Nature,* vol. 489, pp. 128-32, 2012.

[85] N. Stribeck, *X-ray scattering of soft matter*, Springer Science & Business Media, 2007.

[86] B.D. Cullity, "Elements of X-ray diffraction", Addition-Wesley, *Reading, MA,* 1978.

[87] A. Bogner, P. H. Jouneau, G. Thollet, D. Basset, and C. Gauthier, "A history of scanning electron microscopy developments: towards "wet-STEM" imaging", *Micron,* vol. 38, pp. 390-401, 2007.

[88] K. Vernon-Parry, "Scanning electron microscopy: an introduction", *III-Vs Review,* vol. 13, pp. 40-44, 2000.

[89] W. Zhou, R. Apkarian, Z. L. Wang, and D. Joy, "Fundamentals of Scanning Electron Microscopy, in *Scanning Microscopy for Nanotechnology*, ed: Springer, 2006, pp. 1-40.

[90] H. Kohl and L. Reimer, *Transmission Electron Microscopy: Physics of Image Formation*, Springer-Verlag New York, 2008.

[91] D. B. Williams and C. B. Carter, "The transmission electron microscope," in *Transmission electron microscopy*, ed: Springer, 1996, pp. 3-17.

[92] P. C. Braga and D. Ricci, *Atomic force microscopy: biomedical methods and applications*, Springer Science & Business Media, vol. 242, 2004.

[93] P. Eaton and P. West, *Atomic force microscopy*, Oxford University Press, 2010.

[94] C. D. Wagner and G. Muilenberg, *Handbook of X-ray photoelectron spectroscopy*, Perkin-Elmer, 1979.

[95] J. M. Wagner, *X-ray photoelectron spectroscopy,* Nova Science Publishers, 2011.

[96] E. Barsoukov and J. R. Macdonald, *Impedance spectroscopy: theory, experiment, and applications*, John Wiley & Sons, 2005.

[97] V. F. Lvovich, *Impedance spectroscopy: applications to electrochemical and dielectric phenomena*, John Wiley & Sons, 2012.

[98] D. K. Gosser, *Cyclic voltammetry: simulation and analysis of reaction mechanisms*, VCH New York, vol. 43, 1993.

[99] J. Heinze, "Cyclic voltammetry-"Electrochemical spectroscopy". New analytical methods (25)", *Angewandte Chemie International Edition in English,* vol. 23, pp. 831-847, 1984.

[100] S. Dasgupta, G. Stoesser, N. Schweikert, R. Hahn, S. Dehm, R. Kruk, and H. Hahn, "Printed and Electrochemically Gated, High-Mobility, Inorganic Oxide Nanoparticle FETs and Their Suitability for High-Frequency Applications", *Advanced Functional Materials,* vol. 22, pp. 4909-4919, 2012.

[101] R. F. Minibaev, A. A. Bagatur'yants, D. I. Bazhanov, A. A. Knizhnik, and M. V. Alfimov, "First-principles investigation of the electron work function for the (001) surface of indium oxide In_2O_3 and indium tin oxide (ITO) as a function of the surface oxidation level", *Nanotechnologies in Russia,* vol. 5, pp. 185-190, 2010.

[102] H. R. Lillie, "Viscosity of glass between the strain point and melting temperature", *Journal of the American Ceramic Society,* vol. 14, pp. 502-512, 1931.

[103] B. D. Cullity, *Elements of X-ray Diffraction*, Addison-Wesley Company, Inc., 1978.

[104] D. H. Lee, Y. J. Chang, G. S. Herman, and C. H. Chang, "A General Route to Printable High-Mobility Transparent Amorphous Oxide Semiconductors", *Advanced Materials,* vol. 19, pp. 843-847, 2007.

[105] S. E. Oraby, A. M. Alaskari, "Atomic Force Microscopy (AFM) Topographical Surface Characterization of Multilayer-Coated and Uncoated Carbide Inserts", *International Journal of*

Mechanical, Aerospace, Industrial, Mechatronic and Manufacturing Engineering, vol. 4, pp. 977-988, 2010.

[106] K. J. Carroll, J. U. Reveles, M. D. Shultz, S. N. Khanna, and E. E. Carpenter, "Preparation of Elemental Cu and Ni Nanoparticles by the Polyol Method: An Experimental and Theoretical Approach", *The Journal of Physical Chemistry C*, vol. 115, pp. 2656-2664, 2011.

[107] K. Matsuzaki, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, and H. Hosono, "Epitaxial growth of high mobility Cu_2O thin films and application to p-channel thin film transistor", *Applied Physics Letters*, vol. 93, p. 202107, 2008.

[108] R. F. P. Martins, A. Ahnood, N. Correia, L. M. N. P. Pereira, R. Barros, P. M. C. B. Barquinha, R. Costa, I. M. M. Ferreira, A. Nathan, and E. E. M. C. Fortunato, "Recyclable, Flexible, Low-Power Oxide Electronics", *Advanced Functional Materials*, vol. 23, pp. 2153-2161, 2013.

[109] A. P. Chandrakasan and R. W. Brodersen, "Minimizing power consumption in digital CMOS circuits", *Proceedings of the IEEE*, vol. 83, pp. 498-523, 1995.

[110] M. Grouchko, A. Kamyshny, C. F. Mihailescu, D. F. Anghel, and S. Magdassi, "Conductive inks with a "built-in" mechanism that enables sintering at room temperature", *ACS Nano*, vol. 5, pp. 3354-9, 2011.

[111] P. L. Golas, S. Louie, G. V. Lowry, K. Matyjaszewski, and R. D. Tilton, "Comparative Study of Polymeric Stabilizers for Magnetite Nanoparticles Using ATRP", *Langmuir*, vol. 26, pp. 16890-16900, 2010.

[112] W. Z. Wang, G. Wang, X. S. Wang, Y. Zhan, Y. Liu, and C. L. Zheng, "Synthesis and characterization of Cu_2O nanowires by a novel reduction route", *Advanced Materials*, vol. 14, pp. 67-69, 2002.

[113] D. Liyanage, R. J. Thamali, A. Kumbalatara, J. Weliwita, and S. Witharana, "An Analysis of Nanoparticle Settling Times in Liquids", *Journal of Nanomaterials*, vol. 2016, p. 44, 2016.

[114] M. J. Panzer and C. D. Frisbie, "Polymer electrolyte gate dielectric reveals finite windows of high conductivity in organic thin film transistors at high charge carrier densities", *Journal of the American Chemical Society*, vol. 127, pp. 6960-1, 2005.

[115] M. J. Panzer and C. D. Frisbie, "Polymer electrolyte-gated organic field-effect transistors: low-voltage, high-current switches for organic electronics and testbeds for probing electrical transport at high charge carrier density", *Journal of the American Chemical Society*, vol. 129, pp. 6599-607, 2007.

[116] C. Wang, K. Ryu, A. Badmaev, J. Zhang, and C. Zhou, "Metal contact engineering and registration-free fabrication of complementary metal-oxide semiconductor integrated circuits using aligned carbon nanotubes", *ACS Nano*, vol. 5, pp. 1147-53, 2011.

[117] N. J. Tremblay, B. J. Jung, P. Breysse, and H. E. Katz, "Digital Inverter Amine Sensing via Synergistic Responses by n and p Organic Semiconductors", *Advanced Functional Materials*, vol. 21, pp. 4314-4319, 2011.

[118] Y. Li, L. Lan, P. Xiao, Z. Lin, S. Sun, W. Song, E. Song, P. Gao, P. Zhang, and J. Peng, "Facile patterning of amorphous indium oxide thin films based on a gel-like aqueous precursor for low-

temperature, high performance thin-film transistors", *Journal of Materials Chemistry C,* vol. 4, pp. 2072-2078, 2016.

[119] R. A. John, A. C. Nguyen, Y. Chen, S. Shukla, S. Chen, and N. Mathews, "Modulating Cationic Ratios for High-Performance Transparent Solution-Processed Electronics", *ACS Applied Materials & Interfaces,* vol. 8, pp. 1139-46, 2016.

[120] A. Liu, G. Liu, H. Zhu, H. Song, B. Shin, E. Fortunato, R. Martins, and F. Shan, "Water-Induced Scandium Oxide Dielectric for Low-Operating Voltage n- and p-Type Metal-Oxide Thin-Film Transistors", *Advanced Functional Materials,* vol. 25, pp. 7180-7188, 2015.

[121] M.-K. Kim, H. Kang, K. Kang, S.-H. Lee, J. Y. Hwang, Y. Moon, and S.-J. Moon, "Laser sintering of inkjet-printed silver nanoparticles on glass and PET substrates", in *Nanotechnology (IEEE-NANO), 10th IEEE Conference on*, pp. 520-524, 2010.

[122] M. Zenou, O. Ermak, A. Saar, and Z. Kotler, "Laser sintering of copper nanoparticles", *Journal of Physics D: Applied Physics,* vol. 47, p. 025501, 2014.

[123] L. Ming, H. Yang, W. Zhang, X. Zeng, D. Xiong, Z. Xu, H. Wang, W. Chen, X. Xu, M. Wang, J. Duan, Y.-B. Cheng, J. Zhang, Q. Bao, Z. Wei, and S. Yang, "Selective laser sintering of TiO_2 nanoparticle film on plastic conductive substrate for highly efficient flexible dye-sensitized solar cell application", *Journal of Materials Chemistry A,* vol. 2, p. 4566, 2014.

[124] A. Gat, L. Gerzberg, J. F. Gibbons, T. J. Magee, J. Peng, and J. D. Hong, "cw laser anneal of polycrystalline silicon: Crystalline structure, electrical properties", *Applied Physics Letters,* vol. 33, p. 775, 1978.

[125] Y.-H. Yang, S. S. Yang, and K.-S. Chou, "Characteristic enhancement of solution-processed In-Ga-Zn oxide thin-film transistors by laser annealing", *IEEE Electron Device Letters*, vol. 31, pp. 969-971, 2010.

[126] H. Pan, N. Misra, S. H. Ko, C. P. Grigoropoulos, N. Miller, E. E. Haller, and O. Dubon, "Melt-mediated coalescence of solution-deposited ZnO nanoparticles by excimer laser annealing for thin-film transistor fabrication", *Applied Physics A,* vol. 94, pp. 111-115, 2008.

[127] T. Park and D. Kim, "Excimer laser sintering of indium tin oxide nanoparticles for fabricating thin films of variable thickness on flexible substrates", *Thin Solid Films,* vol. 578, pp. 76-82, 2015.

[128] K. L. Parry, A. G. Shard, R. D. Short, R. G. White, J. D. Whittle, and A. Wright, "ARXPS characterisation of plasma polymerised surface chemical gradients", *Surface and Interface Analysis,* vol. 38, pp. 1497-1504, 2006.

[129] J. H. Scofield, "Hartree-Slater subshell photoionization cross-sections at 1254 and 1487 eV", *Journal of Electron Spectroscopy and Related Phenomena,* vol. 8, pp. 129-137, 1976.

[130] S. Tanuma, C. J. Powell, and D. R. Penn, "Calculations of electron inelastic mean free paths. V. Data for 14 organic compounds over the 50–2000 eV range", *Surface and Interface Analysis,* vol. 21, pp. 165-176, 1994.

[131] B. W. Chieng and Y. Y. Loo, "Synthesis of ZnO nanoparticles by modified polyol method", *Materials Letters*, vol. 73, pp. 78-82, 2012.

[132] N. Zydziak, C. Hübner, M. Bruns, C. Barner-Kowollik, "One-step Functionalization of Single-Walled Carbon Nanotubes (SWCNTs) with Cyclopentadienyl Capped Macromolecules via Diels-Alder Chemistry", *Macromolecules*, vol. 44, pp. 3374–3380, 2011.

[133] L. Stolzer, I. Ahmed, C. Rodriguez-Emmenegger, V. Trouillet, P. Bockstaller, C. Barner-Kowollik and L. Fruk, "Light-induced modification of silver nanoparticles with functional polymers", *Chemical Communications*, vol. 50, pp. 4430-4433, 2014.

[134] A. Bourlange, D. J. Payne, R. G. Palgrave, H. Zhang, J. S. Foord, R. G. Egdell, R. M. J. Jacobs, T. D. Veal, P. D. C. King, and C. F. McConville, "The influence of Sn doping on the growth of In_2O_3 on Y-stabilized ZrO_2 (100) by oxygen plasma assisted molecular beam epitaxy", *Journal of Applied Physics*, vol. 106, pp. 013703, 2009.

[135] T. T. Baby, S. K. Garlapati, S. Dehm, M. Häming, R. Kruk, H. Hahn, and S. Dasgupta, "A General Route toward Complete Room Temperature Processing of Printed and High Performance Oxide Electronics", *ACS Nano*, vol. 9, p. 8, 2015.